Rockwell Semiconductor Systems

RCV56HCF
PCI/CardBus Modem Designer's Guide

(Preliminary)

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NOTICE

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1. INTRODUCTION

1.1 SUMMARY

The Rockwell RCV56HCF-PCI Host-Controlled Modem Device Family supports high speed analog data, high speed fax, ISDN, DSVD, AudioSpan, speakerphone, audio/voice, and VoiceView operation. It operates with PSTN or ISDN telephone lines in the U.S. and world-wide and is offered in several device models (see Table 1-1).

The modem device set consists of PC PCI bus interface (BIF) and modem data pump (MDP) hardware available in two thin quad flat packs (TQFPs). Host-controlled modem software is also provided.

Operating with +3.3V power, this device set supports 32-bit host applications in such designs as embedded motherboards, PCI half cards, and CardBus cards.

Figure 1-1 illustrates the general structure of the RCV56HCF software and the interface to the RCV56HCF hardware. Figure 1-2 illustrates the major hardware interfaces supported by each model.

The RCV56HCF employs a downloadable architecture so that the user can update MDP executable code.

Using K56flex™ technology, the RCV56HCF can receive data at speeds up to 56 kbps from a digitally connected K56flex-compatible central site modem, such as a Rockwell RC56CSM modem. K56flex modems take advantage of the PSTN which is primarily digital except for the client modem to central office local loop and are ideal for applications such as remote access to an Internet service provider (ISP), on-line service, or corporate site. The RCV56HCF can send data at speeds up to V.34 rates.

In V.34 data mode, the modem operates at line speeds up to 33600 bps. Error correction (V.42/MNP 2-4) and data compression (V.42 bis/MNP 5) maximize data transfer integrity and boost average data throughput. Non-error-correcting mode is also supported.

AudioSpan (analog simultaneous audio/voice and data) operation supports a data rate with audio of 4.8 kbps.

SP models support position independent, full-duplex speakerphone (FDSP), as well as digital simultaneous voice and data (DSVD) with speech coding per ITU-T G.729 Annex A with interoperable G.729 Annex B, and SIG DigiTalk™ DSVD.

The modem supports fax Group 3 send and receive rates up to 28800 bps and T.30 protocol.

V.80 and Rockwell Video Ready compatible synchronous access modes support host-controlled communication protocols, e. g., H.324 video conferencing.

In voice/audio mode, PCM coding and decoding at 8000 Hz sample rate allows efficient digital storage of voice/audio. This mode supports digital telephone answering machine, voice annotation, and audio recording/playback applications.

AccelerATor kits and reference designs are available to minimize application design time and costs.

This designer's guide describes the modem hardware capabilities and identifies the supporting commands. Commands and parameters are defined in the RCVHCF Command Reference Manual (Order No. 1118).

1.2 FEATURES

- Data modem
  - K56flex, 33.6 kbps, 31.2 kbps, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, and V.21; Bell 212A and 103
  - V.42 LAPM and MNP 2-4 error correction
  - V.42 bis and MNP 5 data compression
  - V.25 ter (Annex A) and EIA 602 command set
- Fax modem send and receive rates up to 28800 bps
  - ITU-T V.34 fax*, V.17, V.29, V.27 ter, and V.21 ch 2
  - EIA/TIA 578 Class 1, Class 1.0 (T.31) fax
- ISDN BRI support (option)*
  - PC Bus support 2B+D channels
  - IOM-2 interface to external U or S/T transceiver
  - Simultaneous transfer of B1, B2, D channels (144 kbps; 64 kbps x 2, 16 kbps)
  - V.34, DSVD, FDSP, audio functions over B channel

- AudioSpan (simultaneous audio/voice and data)*
  - ITU-T V.61 modulation (4.8 kbps data plus audio)
  - Handset, headset, or half-duplex speakerphone
- ITU-T V.70 DSVD (option)
  - ITU-T G.729 Annex A with interoperable G.729 Annex B
  - SIG (special interest group) DigiTalk DSVD
  - Voice/silence detection and handset echo cancellation
  - Handset, headset, or half-duplex speakerphone
- Full-duplex speakerphone (FDSP) mode
  - Over PSTN or ISDN B channel (option)
  - Switching to/from data, fax, DSVD and VoiceView
  - Microphone gain and muting
  - Speaker volume control and muting
  - Adaptive line and acoustic echo cancellation
  - Loop gain control, transmit and receive path AGC
  - Acoustic echo cancellation concurrent with DSVD
  - Noise suppression
  - Room monitor
- V.80 and Rockwell Video Ready synchronous access modes support host-controlled communication protocols
  - H.324 interface support
- V.8/V.8bis and supporting AT commands (V.25 ter with Annex A)
- Data/Fax/VoiceView/Voice call discrimination
- Voice, telephony, audio, VoiceView
  - Voice (8-bit µ-Law compression/decompression)
  - TIA-695 command set
  - VoiceView alternating voice and data (option)
  - 8-bit linear and 8-bit µ-Law record/playback
  - 8.0 kHz, 11.025 kHz, 22.050 kHz and 44.1 kHz (down sampled to 11.025)
  - Handset, acoustic, line echo cancellation
  - Music on hold from host or analog hardware input
  - TAM support with concurrent DTMF detect, ring detect and caller ID
- World-class operation (option)
  - Call progress, blacklisting, multiple country support
- Integrated internal hybrid
- Caller ID and distinctive ring detect
- Modem and audio paths concurrent across PCI bus
- Single profile stored in host
- System compatibilities
  - Windows 95 and Windows NT operating systems
  - Microsoft's PC 97 Design Initiative compliant
  - Unimodem/V compliant
- 32-bit PCI Local Bus interface
  - Conforms to the PCI Local Bus Specification, Production Version, Revision 2.1
  - PCI Bus Mastering interface to the MDP
  - CardBus support with 512-byte RAM for CIS
  - 33 MHz PCI clock support
- Device packages:
  - Bus Interface in 176-pin TQFP
  - MDP in 144-pin TQFP
- +3.3V operation

* See Note 6 in Table 1-1.

Table 1-1. Modem Models and Functions

Marketing Model Number[1]	Supported Functions				
	K56flex, V.34 Fax[6]	Voice/Audio/ VoiceView/ AudioSpan[6]	ISDN[5,6]	Full-duplex Speakerphone (FDSP) and DSVD	W-Class
RCV56HCF/ISDN	Y	Y	Y	Y	–
RCV56HCFW/ISDN	Y	Y	Y	Y	Y
RCV56HCF/SP	Y	Y	–	Y	–
RCV56HCFW/SP	Y	Y	–	Y	Y
RC56HCF	Y	–	–	–	–
RC56HCFW	Y	–	–	–	Y

Notes:

1. The two-device set manufacturing part numbers are:
   PCI Bus Interface in 176-pin TQFP: 11229-XX.
   MDP in 144-pin TQFP: R6776-XX.
2. Legend:
   Y = Function supported.
   – = Function not supported.
3. Model options:
   SP Speakerphone and DSVD.
   V Voice, audio, and VoiceView.
   W World-class (W-class).
4. Supported functions (Y = Supported; – = Not supported):
   FDSP Full-duplex speakerphone.
   DSVD Digital simultaneous voice and data.
   Voice/Audio Voice and audio functions.
   VoiceView VoiceView alternating voice and data.
   W-Class World-class functions supporting multiple country requirements.
5. Provides ISDN functionality with the addition of a U or S/T transceiver device.
6. Initial production does not include support for ISDN, V.34 fax, and AudioSpan.

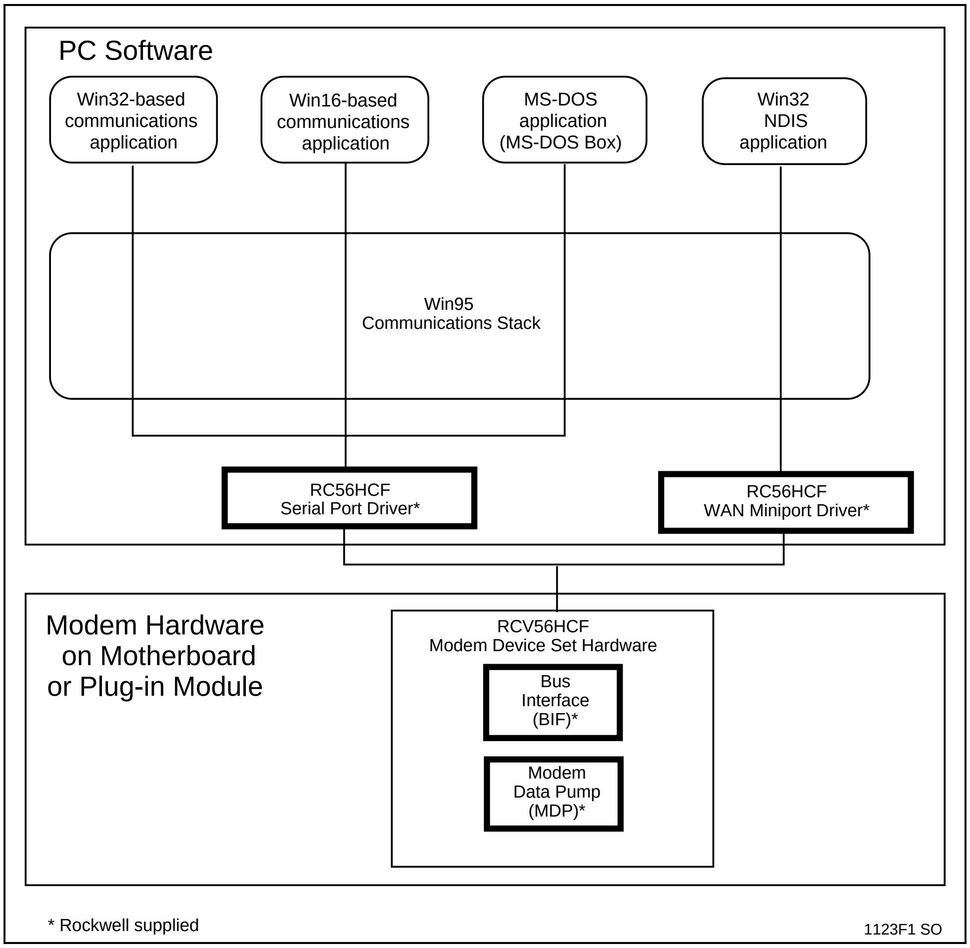


Figure 1-1. RCV56HCF System Overview

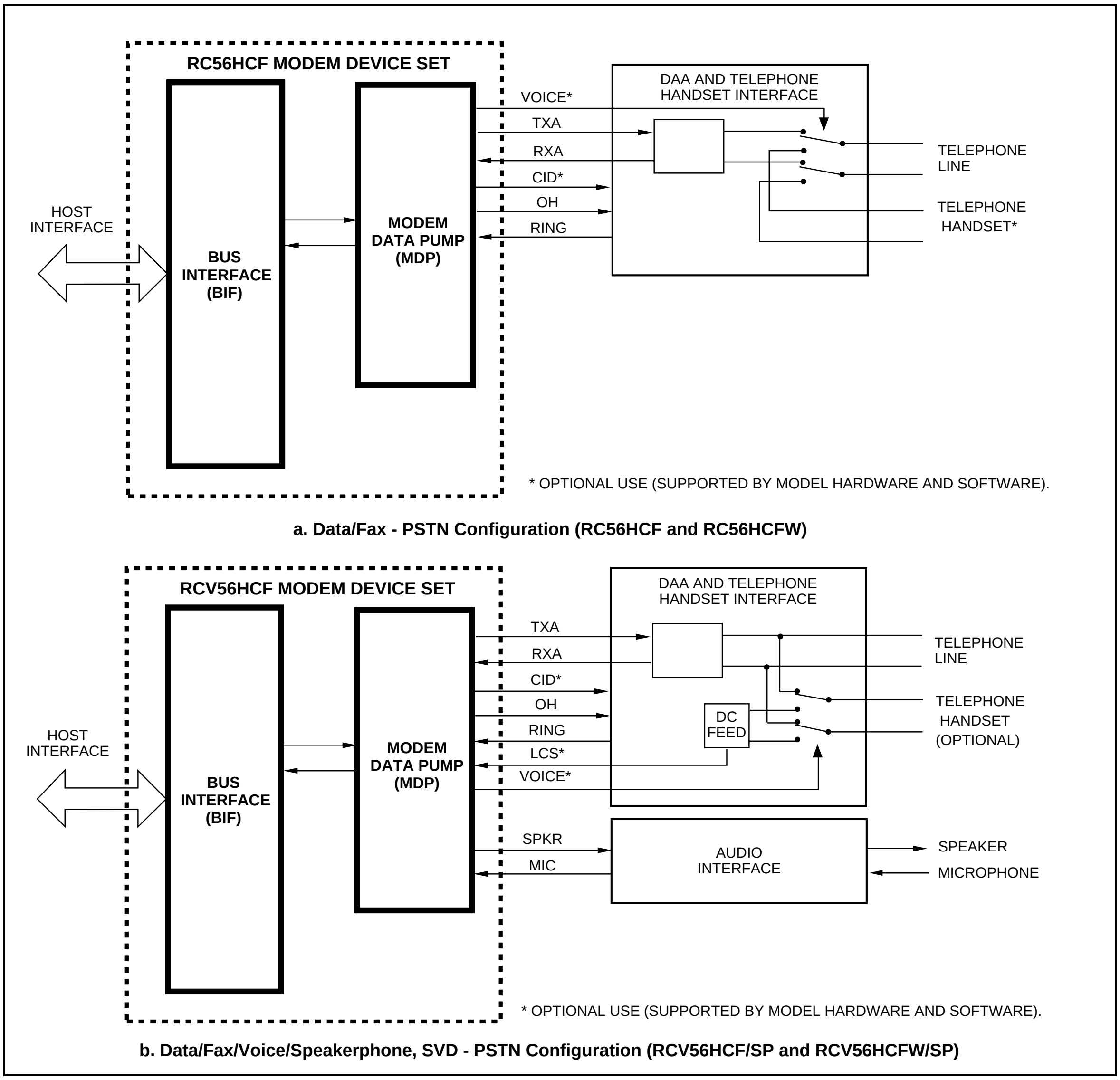
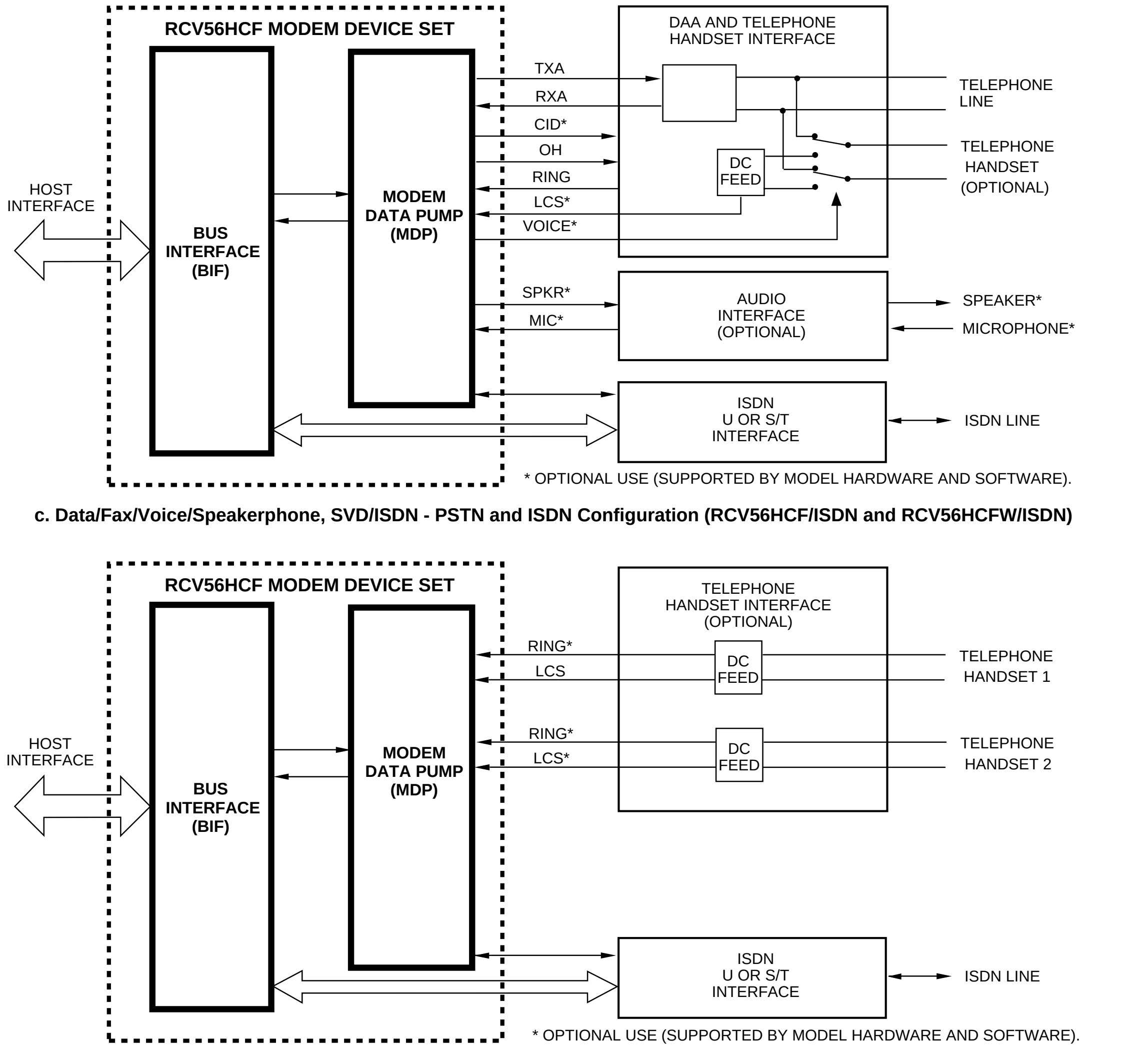


Figure 1-2. RCV56HCF Hardware Configuration Block Diagram



c. Data/Fax/Voice/Speakerphone, SVD/ISDN - PSTN and ISDN Configuration (RCV56HCF/ISDN and RCV56HCFW/ISDN)

d. Data/Fax/Voice/Speakerphone, SVD/ISDN - ISDN Only Configuration (RCV56HCF/ISDN and RCV56HCFW/ISDN)

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Figure 1-2. RCV56HCF Hardware Configuration Block Diagram (Continued)

1.3 TECHNICAL OVERVIEW

1.3.1 General Description

The RCV56HCF Device Set provides the processing core for a complete system design featuring data/fax modem, DSVD, AudioSpan, speakerphone, voice/audio, and VoiceView depending on specific model (Table 1-1). Note: RCV56HCF Device Set refers to the family of single device modem models listed in Table 1-1.

The modem is the full-featured, self-contained data modem/fax modem/DSVD/voice/audio/speakerphone solution. Dialing, call progress, telephone line interface, AudioSpan, DSVD, speakerphone, voice/audio, and VoiceView functions are supported and controlled through the command set.

The modem hardware connects to the host PC via a PCI bus interface. The OEM adds a crystal circuit, telephone line interface, telephone interface (optional), audio interface (optional), and ISDN interface (optional) to complete the system.

1.3.2 Operating Modes

<u>Data/Fax Modes</u>

In K56flex™ mode, the modem can receive data from a digital source using a K56flex™ -compatible central site modem (e. g., Rockwell RC56CSM) over the digital telephone network portion of the PSTN at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at V.34 rates. This mode can fall back to full-duplex V.34 mode, and to slower rates as supported by line conditions.

In V.34 data modem mode, the modem can also operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33600 bps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standard are supported.

In fax modem modes, the modem fully supports Group 3 facsimile send and receive speeds of 28800, 14400, 12000, 9600, 7200, 4800, or 2400 bps. Fax modes support Group 3 fax requirements. Fax data transmission and reception performed by the modem are controlled and monitored through the fax EIA-578 Class 1 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

Both transmit and receive fax data are buffered within the modem. Data transfer to and from the DTE is flow controlled by XON/XOFF and RTS/CTS.

<u>AudioSpan Modes</u>

AudioSpan provides full-duplex analog simultaneous audio/voice and data over a single telephone line at a data rate with audio of 4800 bps using V.61 modulation. AudioSpan can send any type of audio waveform, including music. Data can be sent with or without error correction. The audio/voice interface can be in the form of a headset, handset, or microphone and speaker (half-duplex speakerphone). Handset echo cancellation is provided.

<u>Host-Controlled DSVD Mode (ISDN and SP Models)</u>

ISDN and SP models support host-controlled DSVD. A microphone and a speaker are required.

ITU-T interoperable G.729 and G.729 Annex A with interoperable G.729 Annex B Operation. Voice activity detection supports speech coding at an average bit rate significantly lower than 8.0 kbps.

SIG DigiTalk. Speech coding is performed at 8.5 kbps.

<u>Voice/Audio Mode (V Models)</u>

Voice/Audio Mode features include 8-bit linear and 8-bit µ-Law coding/decoding, tone detection/generation and call discrimination, concurrent DTMF detection, and 8-bit monophonic audio data encoding at 11.025 kHz or 8000 Hz.

Voice/Audio Mode is supported by three submodes:

1. Online Voice Command Mode supports connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset).
2. Voice Receive Mode supports recording voice or audio data input at the MIC_M pin, typically from a microphone/handset or the telephone line.
3. Voice Transmit Mode supports playback of voice or audio data to the TXA1_L1/TXA2_L1 output, typically to a speaker/handset or to the telephone line.

Speakerphone Mode (ISDN and SP Models)

The speakerphone mode features an advanced proprietary speakerphone algorithm which supports full-duplex voice conversation with both acoustic and line echo cancellation. Parameters are constantly adjusted to maintain stability with automatic fallback from full-duplex to pseudo-duplex operation. The speakerphone algorithm allows position independent placement of microphone and speaker.

The speakerphone mode provides hands-free full-duplex telephone operation under host control. The host can separately control volume, muting, and AGC in microphone and speaker channels.

Synchronous Access Mode (SAM)

V.80 and Rockwell Video Ready synchronous access modes between the modem and the host/DTE are provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

1.3.3 Host-Controlled Modem Software

Host-controlled modem software performs processing of general modem control, command sets, fax Class 1, AudioSpan, DSVD, speakerphone, voice/audio/TAM, error correction, data compression, and operating system interface functions. Configurations of the modem software are provided to support modem models listed in Table 1-1.

Binary executable modem software is provided for the OEM.

1.3.4 Downloadable Modem Data Pump Firmware

Binary executable code controlling MDP operation is downloaded as required during operation.

1.3.5 Hardware Interfaces

1.3.5.1 PCI Bus Host Interface

The Bus Interface conforms to the PCI Local Bus Specification, Production Version, Revision 2.1, June 1, 1995. It is a memory slave (burst transactions) and a bus master for PC host memory accesses (burst transactions). Configuration is by PCI configuration protocol.

The following interface signals are supported:

- Address and data
  - 32 bidirectional Address/Data (AD[31-0]; bidirectional
  - Four Bus Command and Byte Enable (CBE [3:0]), bidirectional
  - Bidirectional Parity (PAR); bidirectional
- Interface control
  - Cycle Frame (FRAME#); bidirectional
  - Initiator Ready (IRDY#); bidirectional
  - Target Ready (TRDY#); bidirectional
  - Stop (STOP#); bidirectional
  - Initialization Device Select (IDSEL); input
  - Device Select (DEVSEL#); bidirectional
- Arbitration
  - Request (REQ#); output
  - Grant (GRANT#); input
- Error reporting
  - Parity Error ((PERR#); bidirectional
  - System Error ; bidirectional
- Interrupt
  - Interrupt A (INTA#); output
- System
  - Clock (PCICLK); input
  - Reset (PCIRST#); input
  - Clock Running (CLKRUN#); input

1.3.5.2 Serial EEPROM Interface

A serial EEPROM is required to store the Maximum Latency, Minimum Grant, Device ID, Vendor ID, Subsystem ID, and Subsystem Vendor ID parameters for the PCI Configuration Space Header. The serial EEPROM interface connects to an Microchip 93LC66B, Atmel AT93C66, or equivalent 256 x 16 serial EEPROM. The interface signals are: a serial data input line from the EEPROM (SROMIN), a serial data output line to the EEPROM (SROMOUT), Clock to the EEPROM (SROMCLK), and chip select to the EEPROM (SROMCS). The EEPROM is programmable by the PC via the BIF.

1.3.5.3 Audio Interface

One Speaker output (SPKROUT_M) is provided for an optional OEM-supplied speaker circuit. Two microphone inputs are supported: one for Voice Microphone input (MIC_V) and one for Music Microphone input (MIC_M), e.g., music-on-hold.

The MIC_V and SPKROUT_M lines connect to the handset and speaker to support functions such as AudioSpan headset and speakerphone modes, FDSP, telephone emulation, microphone voice record, speaker voice playback, and call progress monitor.

The MIC_M input can accept an external audio signal to support the music-on-hold function and routes it to the telephone line. If music-on-hold function is not required, the microphone signal can be connected to the MIC_M input to support telephone emulation mode.

The Speaker output (SPKROUT_M) carries the normal speakerphone audio or reflects the received analog signals in the modem.

1.3.5.4 Telephone Line/Telephone/Audio Interface

The Telephone Line/Telephone/Audio Signal Interface can support a 3-relay telephone line interface (Figure 1-3). Signal routing for Voice mode is shown in Table 1-2. Relay positions for VoiceView are shown in Table 1-3.

The following signals are supported:

- A single-ended Receive Analog input (RXA_L1) and a differential Transmit Analog output (TXA1_L1 and TXA2_L1) to the telephone line.
- Off-hook (OH_L1#), Caller ID (CID_L1#), and Voice (VOICE_L1#) relay control outputs.
- A Ring Indicate (IRING_L1) input.
- A Loop Current Sense (LCS) input.
- An input from the telephone microphone (TELIN_L1) and an output to the telephone speaker (TELOUT_L1) are supported in AudioSpan modes. These lines connect voice record/playback and AudioSpan audio to the local handset.

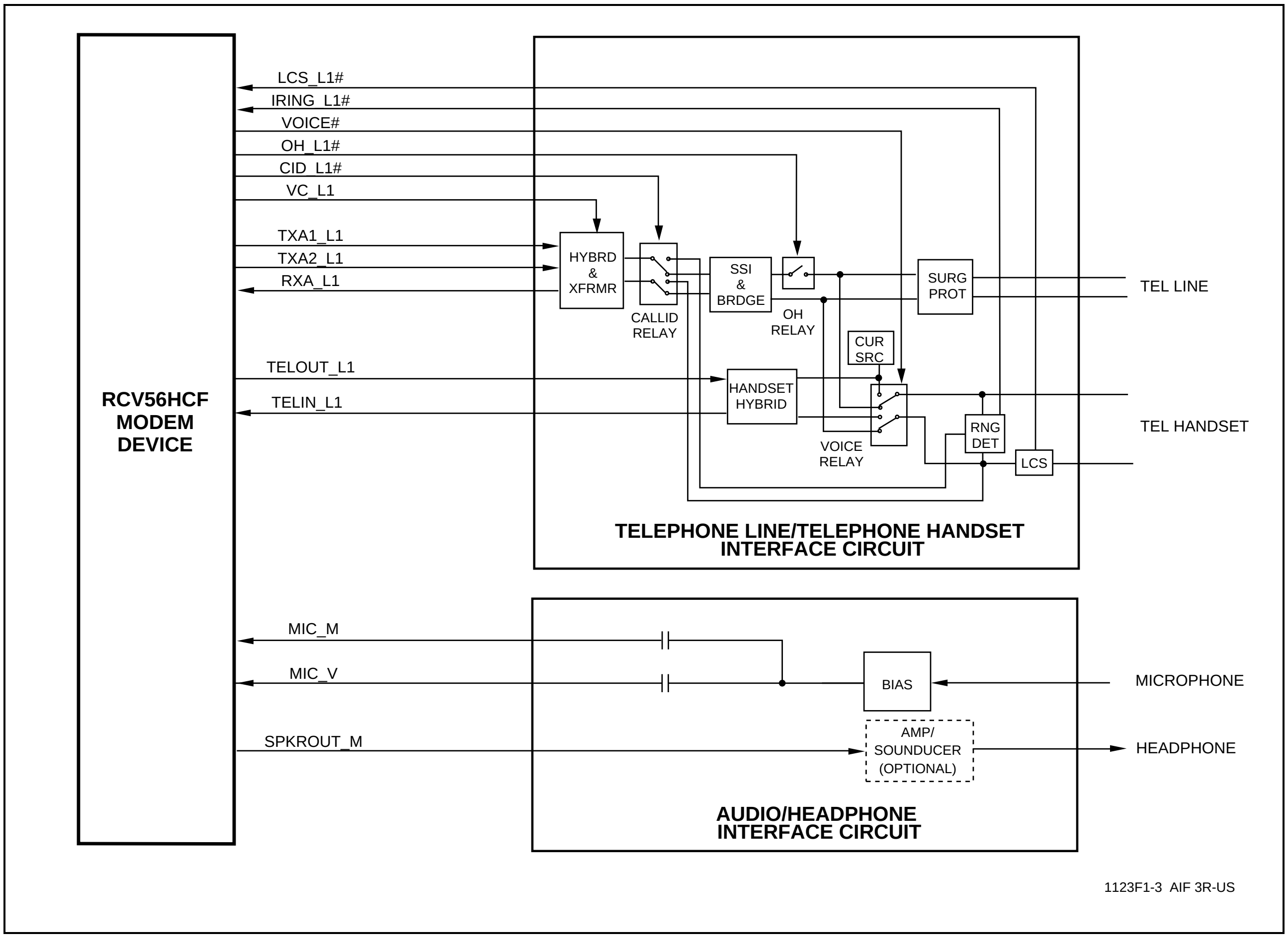


Figure 1-3. Typical Audio Signal Interface (U.S.)

Table 1-2. Typical Signal Routing - Voice Mode

+VLS= Command	Description	Input Selected	Output Selected	OH_L1# Output Activated	VOICE# Output Activated	CID_L1# Output Activated
0	Modem on hook. Phone connected to Line	.	.	No	No	Yes
1	Modem connected to Line.	RXA_L1	TXA1/2_L1	Yes	Yes	No
2	Modem connected to Handset	TELIN_L1	TELOUT_L1	No	Yes	Yes
3	Modem connected to Line and Handset	RXA_L1	TXA	Yes	No	No
4	Modem connected to Speaker		SPKROUT_M	No	No	Yes
5	Modem connected to Line and Speaker	RXA_L1	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
6	Modem connected to Microphone	MIC_V	.	No	No	Yes
7	Speaker and Mic. routed to Line via Modem	RXA_L1, MIC_M	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
8	Modem connected to Speaker	.	SPKROUT_M	No	No	Yes
9	Modem connected to Line and Speaker	RXA_L1	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
10	Speaker and Mic. routed to Line via Modem	RXA_L1, MIC_M	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
11	Modem connected to Microphone	MIC_V	.	No	No	Yes
12	Speaker and Mic. routed to Line via Modem	RXA_L1, MIC_M	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
13	Speaker and Mic. routed to Line via Modem	RXA_L1, MIC_M	TXA1/2_L1, SPKROUT_M	Yes	Yes	No
14	Modem connected to Headset	MIC_V	SPKROUT_M	No	No	Yes
15	Speaker and Mic. routed to Line via Modem	RXA_L1, MIC_M	TXA1/2_L1, SPKROUT_M	Yes	Yes	No

Table 1-3. Relay Positions - VoiceView Mode

2-Relay DAA			
Stage	**Function**	**Off-Hook Relay (OH_L1) Activated**	**Voice Relay (VOICE#) Activated**
1	On-hook	No	No
2a	Detected tone - on-hook	No	No
2b	Detected tone - off-hook for handset and speakerphone	Yes	No
3	Off-hook	Yes	Yes

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2. TECHNICAL SPECIFICATIONS

2.1 ESTABLISHING DATA MODEM CONNECTIONS

Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

Call Progress Tone Detection

Ringback, equipment busy, and progress tones can be detected in accordance with the applicable standard.

Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

Ring Detection

A ring signal can be detected from a TTL-compatible square wave input (frequency is country-dependent).

Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for a period of time determined by country requirement to allow transmission of the billing signal.

Connection Speeds

Data modem line connection can be selected using the +MS command in accordance with V.25 ter. The +MS command selects modulation, enables/disables automode, and selects transmit and receive minimum and maximum line speeds.

Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with V.25 ter.

2.2 DATA MODE

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

DTE-to-Modem Flow Control

If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

Escape Sequence Detection

The "+++" escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

GSTN Cleardown (K56flex, V.34, V.32 bis, V.32)

Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Fall Forward/Fallback (K56flex, V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within K56flex/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS command.

When connected in K56flex/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E1 command.

Retrain

The modem may lose synchronization with the received line signal under poor line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

2.3 ERROR CORRECTION AND DATA COMPRESSION

V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

V.42 bis Data Compression

V.42 bis data compression mode operates when a LAPM or MNP connection is established.

The V.42 bis data compression employs a "string learning" algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two dictionaries, dynamically updated during normal operation, are used to store the strings.

MNP 5 Data Compression

MNP 5 data compression mode operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.4 MNP 10EC™ ENHANCED CELLULAR CONNECTION

A traditional landline modem, when used for high-speed cellular data transmission, typically encounters frequent signal interference and degradation in the connection due to the characteristics of the analog cellular network. In this case, cellular-specific network impairments, such as non-linear distortion, fading, hand-offs, and high signal-to-noise ratio, contribute to an unreliable connection and lower data transfer performance. Implementations relying solely on protocol layer methods, such as MNP 10, generally cannot compensate for the landline modem's degraded cellular channel performance.

The modem achieves higher cellular performance by implementing enhanced cellular connection techniques at both the physical and protocol layers, depending on modem model. The modem enhances the physical layer within the modulation by optimizing its responses to sudden changes in the cellular connection. The MNP 10EC protocol layer implemented in the modem software improves data error identification/correction and maximizes data throughput by dynamically adjusting speed and packet size based on signal quality and data error performance.

2.5 FAX CLASS 1 OPERATION

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.6 VOICE/AUDIO MODE

Voice and audio functions are supported by the Voice Mode. Voice Mode includes three submodes: Online Voice Command Mode, Voice Receive Mode, and Voice Transmit Mode.

2.6.1 Online Voice Command Mode

This mode results from the connection to the telephone line or a voice/audio I/O device (e.g., microphone, speaker, or handset) through the use of the +FCLASS=8 and +VLS commands. After mode entry, AT commands can be entered without aborting the connection.

2.6.2 Voice Receive Mode

This mode is entered when the +VRX command is active in order to record voice or audio data input at the RXA_L1 pin, typically from a microphone/handset or the telephone line.

Received analog voice samples are converted to digital form and compressed for reading by the host. AT commands control the codec bits-per-sample rate.

Received analog mono audio samples are converted to digital form and formatted into 8-bit unsigned linear or µ-Law PCM format for reading by the host. AT commands control the bit length and sampling rate. Concurrent DTMF/tone detection is available.

2.6.3 Voice Transmit Mode

This mode is entered when the +VTX command is active in order to playback voice or audio data to the TXA1_L1 output, typically to a speaker/handset or to the telephone line. Digitized audio data is converted to analog form then output to the TXA1_L1 output.

2.6.4 Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the configuration status. In Tone Mode, all three tone detectors are operational.

2.6.5 Speakerphone Modes

Speakerphone modes are selected in voice mode with the following commands:

Speakerphone ON/OFF (+VSP). This command turns the Speakerphone function ON (+VSP = 1) or OFF (+VSP = 0).

Microphone Gain (+VGM)=<gain>. This command sets the microphone gain of the Speakerphone function. <gain> is an unsigned octet where values greater than 128 indicate a gain larger than nominal and values smaller than 128 indicate a gain smaller than nominal.

Speaker Gain (+VGS=<gain>). This command sets the speaker gain of the Speakerphone function. <gain> is an unsigned octet where values greater than 128 indicate a gain larger than nominal and values smaller than 128 indicate a gain smaller than normal.

2.7 SIMULTANEOUS AUDIO/VOICE AND DATA (AudioSpan)

The modem can operate in AudioSpan Mode if the remote modem is also configured for AudioSpan Mode operation.

AT commands are used to select the AudioSpan Mode, to enable automatic AudioSpan modulation selection or select a specific AudioSpan modulation, and to enable AudioSpan data burst operation.

V.61 modulation supports 4800 bps data speed with audio, and a data-only speed of 4800 bps.

The AudioSpan audio interface defaults to the local handset connected to the modem and can be configured to interface through the modem microphone and speaker pins to support use of a headset or a speakerphone.

2.8 HOST-BASED DSVD MODE

Host-based DSVD operation is enabled by the -SSE or -SMS command. In Host-based DSVD Mode, the modem supports the transfer of data and voice occurs simultaneously during a data connection.

2.9 FULL-DUPLEX SPEAKERPHONE (FDSP) MODE

The modem operates in FDSP mode when +FCLASS=8 and +VSP=1 (see 2.6.5).

In FDSP Mode, speech from a microphone or handset is converted to digital form, shaped, and output to the telephone line through the line interface circuit. Speech received from the telephone line is shaped, converted to analog form, and output to the speaker or handset. Shaping includes both acoustic and line echo cancellation.

2.10 VOICEVIEW

Voice and data can be alternately sent and received in a time-multiplexed fashion over the telephone line whenever the +FCLASS=80 command is active. This command and other VoiceView commands embedded in host communications

software control modem operation. Most VoiceView commands use an extended syntax starting with the characters "-S", which signifies the capability to switch between voice and data.

2.11 CALLER ID

Caller ID can be enabled/disabled using the +VCID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

2.12 WORLD CLASS COUNTRY SUPPORT

The W-class models include functions which support modem operation in multiple countries. The following capabilities are provided in addition to the data modem functions previously described. Country dependent parameters are included in the .INF file for customization by the OEM.

2.12.1 Programmable Parameters

The following parameters are programmable:

- Dial tone detection levels and frequency ranges.
- DTMF dialing transmit output level, DTMF signal duration, and DTMF interdigit interval parameters.
- Pulse dialing parameters such as make/break times, set/clear times, and dial codes.
- Ring detection frequency range.
- Blind dialing disable/enable.
- The maximum, minimum, and default carrier transmit level values.
- Calling tone, generated in accordance with V.25, may also be disabled.
- Call progress frequency and tone cadence for busy, ringback, congested, dial tone 1, and dial tone 2.
- Answer tone detection period.
- On-hook/off-hook, make/break, and set/clear relay control parameters.

2.12.2 Blacklist Parameters

The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted"). Up to 20 such numbers may be tabulated. The blacklist parameters are programmable.

2.13 DIAGNOSTICS

2.13.1 Commanded Tests

Diagnostics are performed in response to &T commands per V.54.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

Analog Loopback with Self Test (&T8 Command). An internally generated test pattern of alternating 1s and 0s (reversals) is sent to the modem. An error detector within the modem checks for errors in the string of reversals.

Remote Digital Loopback (RDL) (&T6 Command). Data from the local DTE is sent to the remote modem which loops the data back to the local DTE.

Remote Digital Loopback with Self Test (&T7 Command). An internally generated pattern is sent from the local modem to the remote modem, which loops the data back to the local modem.

Local Digital Loopback (&T3 Command). When local digital loop is requested by the local DTE, two data paths are set up in the local modem. Data from the local DTE is looped back to the local DTE (path 1) and data received from the remote modem is looped back to the remote modem (path 2).

2.13.2 Power On Reset Tests

Upon power on, an MDP test is performed. If the MDP is not operational, an error indication is generated.

2.14 LOW POWER SLEEP MODE

When not being used, the MDP is placed in a low power state.

3. HARDWARE INTERFACE

3.1 HARDWARE SIGNAL PINS AND DEFINITIONS

The RCV56HCF (PCI) functional interface signals are shown in Figure 3-1.

The Bus Interface hardware interface signals are shown by major interface in Figure 3-2.

The Bus Interface pin assignments for the 176-pin TQFP are shown Figure 3-3 and are listed Table 3-1.

The Bus Interface hardware interface signals are defined in Table 3-2.

The MDP hardware interface signals are shown by major interface in Figure 3-4.

The MDP pin assignments for the 144-pin TQFP are shown in Figure 3-5 and are listed in Table 3-3.

The MDP hardware interface signals are defined in Table 3-4.

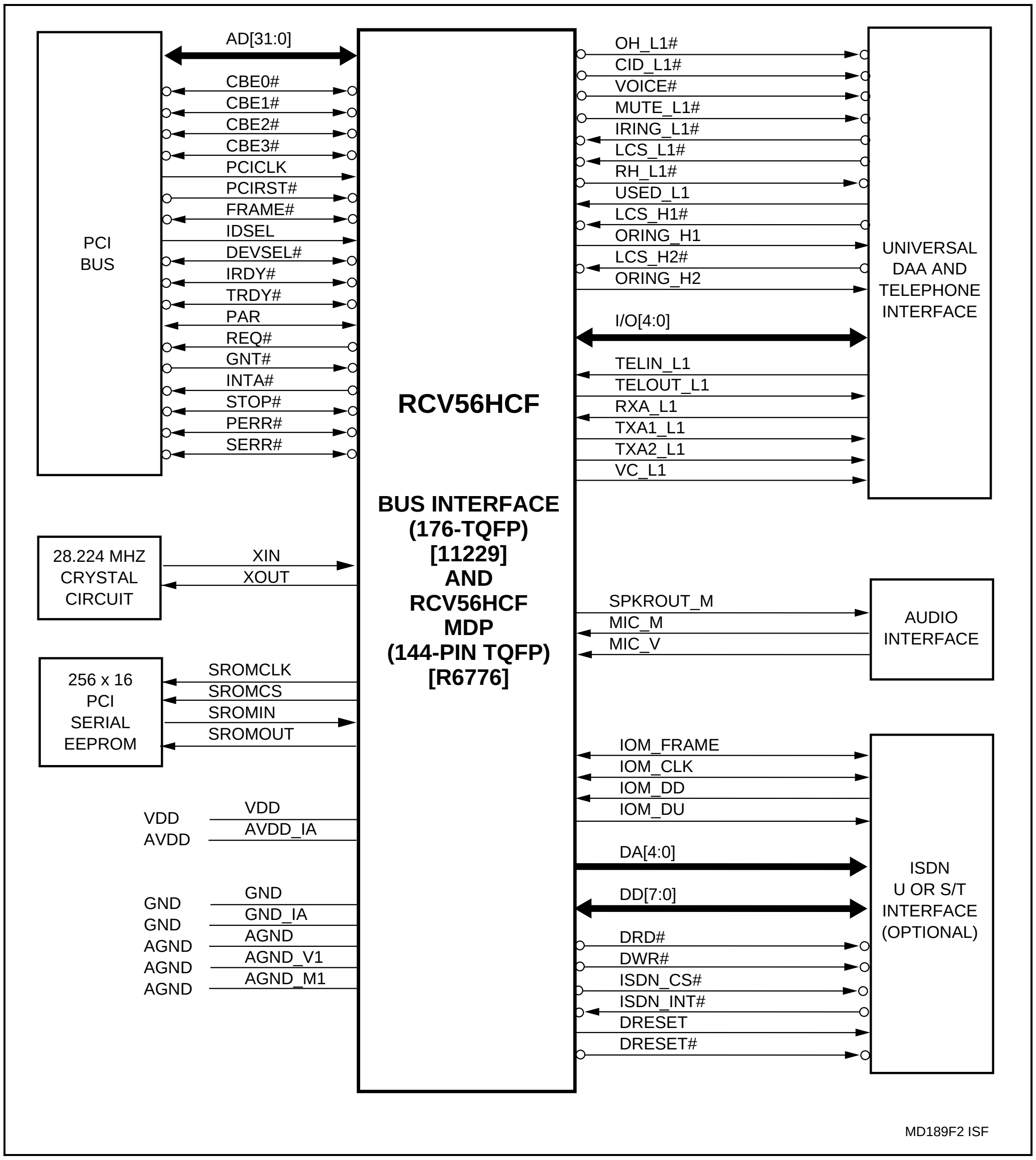


Figure 3-1. RCV56HCF Interface Signals

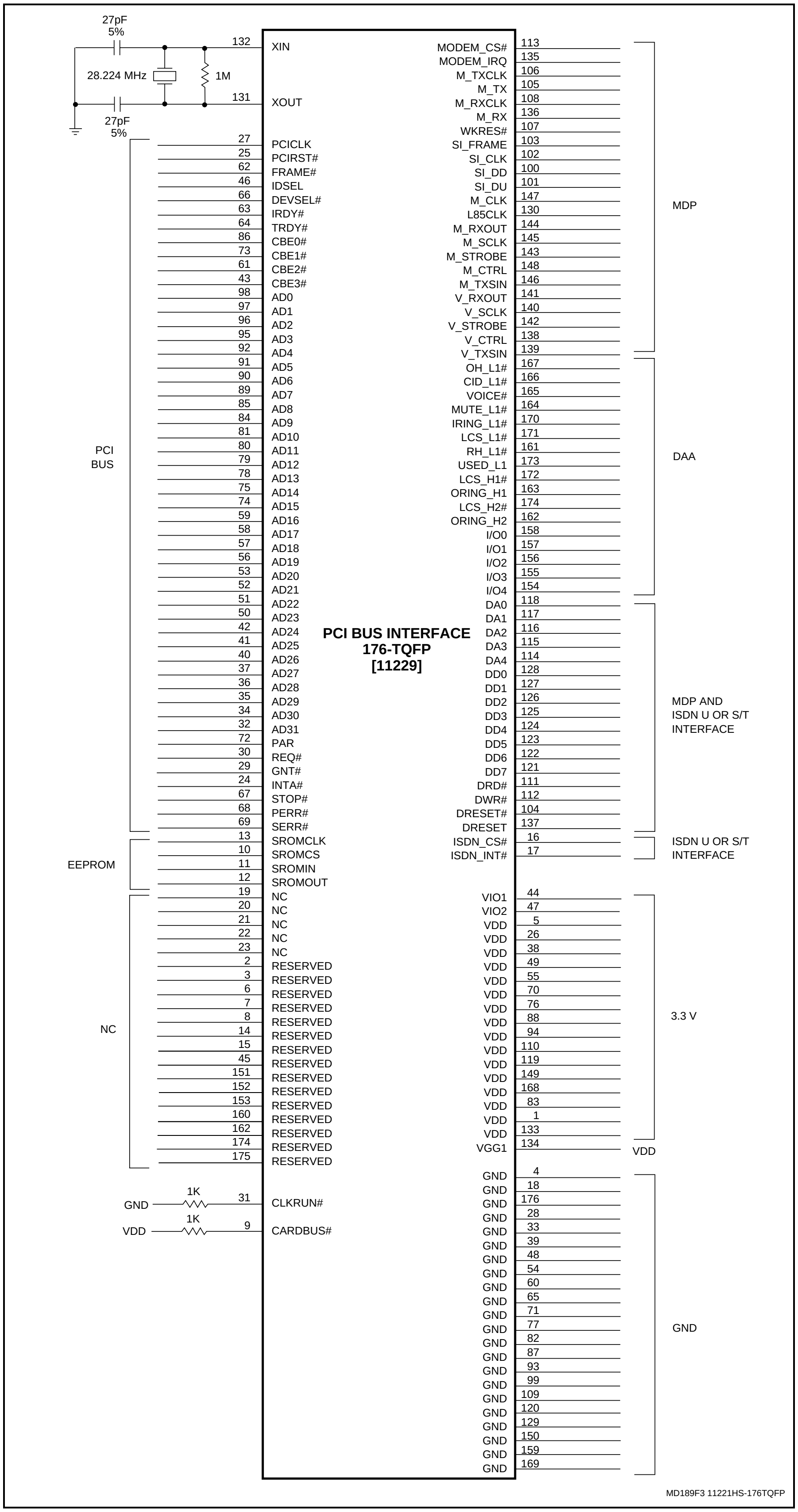


Figure 3-2. Bus Interface 176-Pin TQFP Hardware Interface Signals

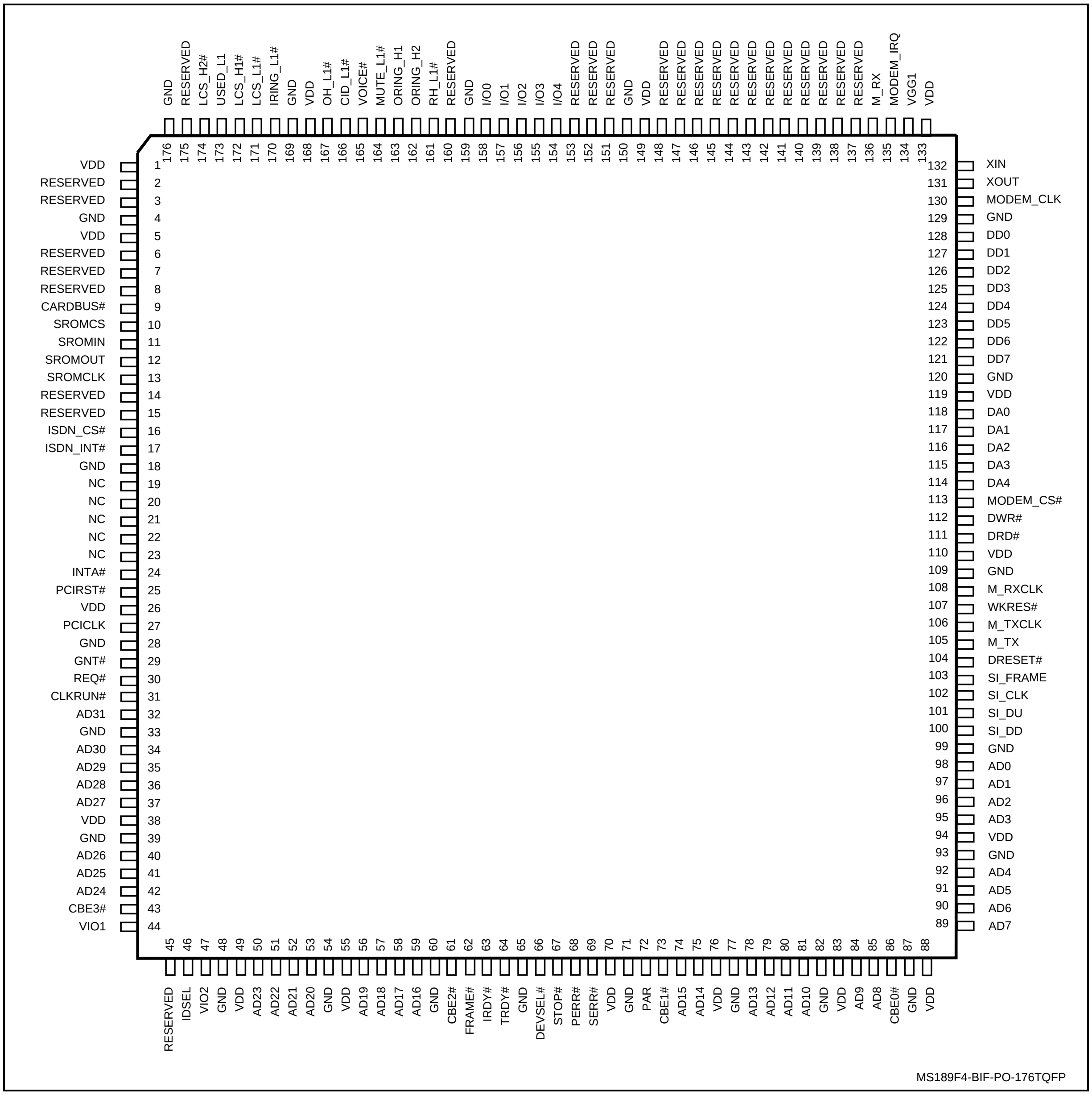


Figure 3-3. Bus Interface 176-Pin TQFP Pin Signals

Table 3-1. Bus Interface 176-Pin TQFP Pin Signals

Pin	Signal Label	I/O	I/O Type[1]	Interface	Pin	Signal Label	I/O	I/O Type[1]	Interface
1	VDD	P	PWR	To 3.3V	89	AD7	I/O	I/Opts	PCI Bus: AD7
2	RESERVED	I	It	To GND	90	AD6	I/O	I/Opts	PCI Bus: AD6
3	RESERVED	I	It	To GND	91	AD5	I/O	I/Opts	PCI Bus: AD5
4	GND	G	GND	Ground	92	AD4	I/O	I/Opts	PCI Bus: AD4
5	VDD	P	PWR	To 3.3V	93	GND	G	GND	Ground
6	RESERVED	O	Ot2	NC	94	VDD	P	PWR	To 3.3V
7	RESERVED	O	Ot2	NC	95	AD3	I/O	I/Opts	PCI Bus: AD3
8	RESERVED	O	Ot2	NC	96	AD2	I/O	I/Opts	PCI Bus: AD2
9	CARDBUS#	I	PWR	VCC through 10KΩ for PCI	97	AD1	I/O	I/Opts	PCI Bus: AD1
10	SROMCS	O	Ot2	SROM Chip Select	98	AD0	I/O	I/Opts	PCI Bus: AD0
11	SROMOUT	O	Ot2	SROM Data Out	99	GND	G	GND	Ground
12	SROMIN	I	It	SROM Data In	100	SI_DD	I	It	MDP: SI Data Downstream
13	SROMCLK	O	Ot2	SROM Clock	101	SI_DU	O	Ot2	MDP: SI Data Upstream
14	RESERVED	O	Ot2	NC	102	SI_CLK	I/O	It/Ot	MDP: SI Clock
15	RESERVED	I	It	To GND	103	SI_FRAME	I/O	It/Ot	MDP: SI Frame
16	ISDN_CS#	O	Ot2	ISDN: CS# or NC	104	DRESET#	O	Ot2	DB: DRESET#
17	ISDN_INT#	I	It	ISDN: IRQ or to GND	105	M_TX	O	Ot2	MDP: M_TX
18	GND	G	GND	Ground	106	M_TXCLK	I	It	MDP: M_RXCLK
19	NC	I	Itpd	NC	107	WKRES#	O	Ot12	Wakeup Reset
20	NC	I	It	NC	108	M_RXCLK	I	It	MDP: M_RXCLK
21	NC	I	It	NC	109	GND	G	GND	Ground
22	NC	O	Ot4ts	NC	110	VDD	P	PWR	To 3.3V
23	NC	I	It	NC	111	DRD#	O	Ot2	DB: DRD#
24	INTA#	O	Opod	PCI Bus: INTA#	112	DWR#	O	Ot2	DB: DWR#
25	PCIRST#	I	Ip	PCI Bus: PCIRST#	113	MODEM_CS#	O	Ot2	MDP: CS#
26	VDD	P	PWR	To 3.3V	114	DA4	O	Ot2	DB: DA4
27	PCICLK	I	Ip	PCI Bus: PCICLK	115	DA3	O	Ot2	DB: DA3
28	GND	G	GND	Ground	116	DA2	O	Ot2	DB: DA2
29	GNT#	I	Ipts	PCI Bus: GNT#	117	DA1	O	Ot2	DB: DA1
30	REQ#	O	Opts	PCI Bus: REQ#	118	DA0	O	Ot2	DB: DA0
31	CLKRUN#	I	It	GND through 1K	119	VDD	P	PWR	To 3.3V
32	AD31	I/O	I/Opts	PCI Bus: AD31	120	GND	G	GND	Ground
33	GND	G	GND	Ground	121	DD7	I/O	It/Ot2	DB: DD7
34	AD30	I/O	I/Opts	PCI Bus: AD30	122	DD6	I/O	It/Ot2	DB: DD6
35	AD29	I/O	I/Opts	PCI Bus: AD29	123	DD5	I/O	It/Ot2	DB: DD5
36	AD28	I/O	I/Opts	PCI Bus: AD28	124	DD4	I/O	It/Ot2	DB: DD4
37	AD27	I/O	I/Opts	PCI Bus: AD27	125	DD3	I/O	It/Ot2	DB: DD3
38	VDD	P	PWR	To 3.3V	126	DD2	I/O	It/Ot2	DB: DD2
39	GND	G	GND	Ground	127	DD1	I/O	It/Ot2	DB: DD1
40	AD26	I/O	I/Opts	PCI Bus: AD26	128	DD0	I/O	It/Ot2	DB: DD0
41	AD25	I/O	I/Opts	PCI Bus: AD25	129	GND	G	GND	Ground
42	AD24	I/O	I/Opts	PCI Bus: AD24	130	MODEM_CLK	O	Ot2	MDP:XTLI
43	CBE3#	I/O	I/Opts	PCI Bus: CBE3#	131	XOUT	O	Ot2	Crystal Output
44	VIO1	P	PWR	To VIO	132	XIN	I	It	Crystal Input
45	RESERVED	I	Itpd	NC	133	VDD	P	PWR	To 3.3V
46	IDSEL	I	Ip	PCI Bus: IDSEL	134	VGG1	P	PWR	To VDD or 3.3V
47	VIO2	P	PWR	To VIO	135	MODEM_IRQ	I	It	MDP: IRQ#
48	GND	G	GND	Ground	136	M_RX	I	It	MDP: M_RX
49	VDD	P	PWR	To 3.3V	137	MSWRESET	O	Ot2	NC
50	AD23	I/O	I/Opts	PCI Bus: AD23	138	RESERVED	O	Ot2	NC
51	AD22	I/O	I/Opts	PCI Bus: AD22	139	RESERVED	O	Ot	NC
52	AD21	I/O	I/Opts	PCI Bus: AD21	140	RESERVED	I	It	To GND
53	AD20	I/O	I/Opts	PCI Bus: AD20	141	RESERVED	I	It2	To GND
54	GND	G	GND	Ground	142	RESERVED	I	It	To GND
55	VDD	P	PWR	To 3.3V	143	RESERVED	I	It	To GND
56	AD19	I/O	I/Opts	PCI Bus: AD19	144	RESERVED	I	It2	To GND
57	AD18	I/O	I/Opts	PCI Bus: AD18	145	RESERVED	I	It	To GND
58	AD17	I/O	I/Opts	PCI Bus: AD17	146	RESERVED	O	Ot2	NC
59	AD16	I/O	I/Opts	PCI Bus: AD16	147	RESERVED	O	Ot2	NC
60	GND	G	GND	Ground	148	RESERVED	O	Ot2	NC
61	CBE2#	I/O	I/Opts	PCI Bus: CBE2#	149	VDD	P	PWR	To 3.3V
62	FRAME#	I/O	I/Opsts	PCI Bus: FRAME#	150	GND	G	GND	Ground
63	IRDY#	I/O	I/Opsts	PCI Bus: IRDY#	151	RESERVED	I	Itpd	NC
64	TRDY#	I/O	I/Opsts	PCI Bus: TRDY#	152	RESERVED	I/O	It/Ot12	To 3.3V through 47K

Table 3-1. Bus Interface 176-Pin TQFP Pin Signals

Pin	Signal Label	I/O	I/O Type[1]	Interface	Pin	Signal Label	I/O	I/O Type[1]	Interface
65	GND	G	GND	Ground	153	RESERVED	I/O	It/Ot12	To 3.3V through 47K
66	DEVSEL#	I/O	I/Opsts	PCI Bus: DEVSEL#	154	I/O4	I/O	It/Ot12	DAA: Reserved
67	STOP#	I/O	I/Opsts	PCI Bus: STOP#	155	I/O3	I/O	It/Ot12	DAA: Reserved
68	PERR#	I/O	I/Osts	PCI Bus: PERR#	156	I/O2	I/O	It/Ot12	DAA: Reserved
69	SERR#	I/O	I/Opod	PCI Bus: SERR#	157	I/O1	I/O	It/Ot12	DAA: Reserved
70	VDD	P	PWR	To 3.3V	158	I/O0	I/O	It/Ot12	DAA: Reserved
71	GND	G	GND	Ground	159	GND	G	GND	Ground
72	PAR	I/O	I/Opts	PCI Bus: PAR	160	RESERVED	I/O	It/Ot12	To 3.3V through 47K
73	CBE1#	I/O	I/Opts	PCI Bus: CBE1#	161	RH_L1#	O	Ot12	HS: RH
74	AD15	I/O	I/Opts	PCI Bus: AD15	162	ORING_H2	O	Ot12	
75	AD14	I/O	I/Opts	PCI Bus: AD14	163	ORING_H1	O	Ot12	Ring Output Handset
76	VDD	P	PWR	To 3.3V	164	MUTE_L1#	O	Ot12	DAA: Mute Relay
77	GND	G	GND	Ground	165	VOICE#	O	Ot12	DAA: Voice Relay
78	AD13	I/O	I/Opts	PCI Bus: AD13	166	CID_L1#	O	Ot12	DAA: Caller ID Relay
79	AD12	I/O	I/Opts	PCI Bus: AD12	167	OH_L1#	O	Ot12	DAA: Off-Hook Relay
80	AD11	I/O	I/Opts	PCI Bus: AD11	168	VDD	P	PWR	To 3.3V
81	AD10	I/O	I/Opts	PCI Bus: AD10	169	GND	G	GND	Ground
82	GND	G	GND	Ground	170	IRING_L1#	I	It	DAA: Ring Indicate
83	VDD	P	PWR	To 3.3V	171	LCS_L1#	I	It	DAA: Line Current Sense
84	AD9	I/O	I/Opts	PCI Bus: AD9	172	LCS_H1#	I	It	HS: Line Current Sense Handset
85	AD8	I/O	I/Opts	PCI Bus: AD8	173	USED_L1	I	It	
86	CBE0#	I/O	I/Opts	PCI Bus: CBE0#	174	LCS_H2#	I	It	DAA: Line Current Sense
87	GND	G	GND	Ground	175	RESERVED	I	It	To 3.3V through 47K
88	VDD	P	PWR	To 3.3V	176	GND	G	GND	Ground

Notes:

1. I/O types:

I/Opod	Input/Output, PCI, open drain (PCI type =o/d)
I/Opsts	Input/Output, PCI, sustained tristate (PCI type = s/t/s)
I/Opts	Input/Output, PCI, tristate (PCI type = t/s)
Ip	Input, PCI, totem pole (PCI type = in)
Ipts	Input, PCI (PCI type = t/s)
It	Input, TTL
It2	Input, TTL, 2 mA
Itpd	Input, TTL, internal pull-down
It/Ot	Input, TTL/Output, TTL
It/Ot12	Input, TTL/Output, TTL, 12 mA
Opod	Output, PCI, open drain (PCI type =o/d)
Opts	Output, PCI, tristate (PCI type = t/s)
Ot	Output, TTL
Ot2	Output, TTL, 2 mA
Ot4	Output, TTL, 4 mA
Ot12	Output, TTL, 12 mA

2. NC = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump

Table 3-2. Bus Interface Pin Signal Definitions

Label	I/O Type	Signal Name/Description
SYSTEM		
XIN, XOUT	It Ot2	**Crystal In and Crystal Out.** Connect XIN and XOUT to a 28.224 MHz external crystal circuit.
VDD	PWR	**Digital Supply Voltage.** Connect to 3.3V.
GND	GND	**Digital Ground.** Connect to digital ground.
CARDBUS#	It	**CardBus Interface Select.** Selects CardBus (low) or PCI Bus (high) drive strength. For PCI Bus, connect to VCC through 1K ohm.
VGG1	PWR	**I/O Voltage Tolerance Reference.** Connect to VCC.
VIO	PWR	**I/O Signaling Voltage Source.** Connect to 3.3V.
PCI BUS INTERFACE		
PCICLK	Ip (in)	**PCI Bus Clock.** The PCICLK (PCI Bus CLK signal) input provides timing for all transactions on PCI.
CLKRUN#	Ip, (in, o/d, s/t/s)	**Clock Running.** CLKRUN# is an input used to determine the status of CLK and an open drain output used to request starting or speeding up CLK. Connect to GND through 1KΩ for PCI designs.
PCIRST#	Ip (in)	**PCI Bus Reset.** PCIRST# (PCI Bus RST# signal) is used to bring PCI-specific registers, sequencers, and signals to a consistent state.
AD[31:0]	I/Opts (t/s)	**Multiplexed Address and Data.** Address and Data are multiplexed on the same PCI pins.
CBE[3:0]#	I/Opts (t/s)	**Bus Command and Bus Enable.** Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# are used as Byte Enables.
PAR	I/Opts (t/s)	**Parity.** Parity is even parity across AD[31::00] and C/BE[3::0]#. The master drives PAR for address and write data phases; the Bus Interface drives PAR for read data phases.
FRAME#	I/Opsts (s/t/s)	**Cycle Frame.** FRAME# is driven by the current master to indicate the beginning and duration of an access.
IRDY#	I/Opsts (s/t/s)	**Initiator Ready.** IRDY# is used to indicate the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.
TRDY#	I/Opsts (s/t/s)	**Target Ready.** TRDY# is used to indicate s the Bus Interface's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.
STOP#	I/Opsts (s/t/s)	**Stop.** STOP# is asserted to indicate the Bus Interface is requesting the master to stop the current transaction.
IDSEL	Ip (in)	**Initialization Device.** IDSEL input is used as a chip select during configuration read and write transactions.
DEVSEL#	I/Opsts (s/t/s)	**Device Select.** When actively driven, DEVSEL# indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
TRDY#	I/Opts (t/s)	**Reques**t. TRDY# is used to indicate to the arbiter that this agent desires use of the bus.
GNT#	I/Opts (t/s)	**Grant.** GNT# is used to indicate to the agent that access to the bus has been granted.

Table 3-2. Bus Interface Pin Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
PCI BUS INTERFACE (CONTINUED)		
PERR#	I/Opsts (s/t/s)	**Parity Error.** PERR# is used for the reporting of data parity errors.
SERR#	Ood (o/d)	**System Error.** SERR# is an open drain output asserted to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
INTA#	Ood (o/d)	**Interrupt A.** INTA# is an open drain output asserted to request an interrupt.
SERIAL EEPROM INTERFACE (NMC93C56 OR EQUIVALENT)		
SROMCLK	Ot2	**Serial ROM Shift Clock.** Connect to SROM SK input.
SROMCS	Ot2	**Serial ROM Chip Select.** Connect to SROM CS input.
SROMIN	It	**Serial ROM Instruction, Address, and Data In.** Connect to SROM DO output.
SROMOUT	Ot2	**Serial ROM Device Status and Data Out.** Connect to SROM DI input.
DAA INTERFACE		
OH_L1#	Ot12	**Off-Hook Relay Control.** Output (typically active low) used to control the normally open off-hook relay. The polarity of this output is configurable.
CID_L1#	Ot12	**Caller ID Relay Control.** Output (typically active low) used to control the normally open Caller ID relay. The polarity of this output is configurable.
VOICE#	Ot12	**Voice Relay Control.** Output (typically active low) used to control the normally open. The polarity of this output is configurable.
MUTE_L1#	Ot12	**Mute Relay Control.** Output (typically active low) used to control the normally open mute relay. The polarity of this output is configurable.
IRING_L1#	It	**Ring Indicate.** A high-going edge used to initiate presence of a ring frequency. Typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be low.
LCS_L1#	It	**Line Current Sense.** Active low input used to indicate handset off-hook status.
RH_L1#	It	**Remote Hangup.** Active low input used to indicate hangup of the remote modem or telephone, i.e. the remote modem/telephone has released the line (gone on-hook).
USED_L1	Ot12	**Extension Offhook.** Active high input used to indicate the telephone line is in use by the local handset or an extension phone.
LCS_H1#	It	**Line Current Sense Handset 1.** Active low input used to indicate off-hook status from handset 1.
ORING_H1	Ot12	**Ring Output Handset 1.** Active high output used to indicate ring signal to handset 1.
LCS_H2#	It	**Line Current Sense Handset 2.** Active low input used to indicate off-hook status from handset 2.
ORING_H2	Ot12	**Ring Output Handset 2.** Active high output used to indicate ring signal to handset 2.
I/O0-I/O4	It/Ot12	**Reserved.**

Table 3-2. Bus Interface Pin Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
MDP INTERFACE		
DA0-DA4	Ot2	**Device Bus Address Lines 0-4.** Connect to the MDP RS0-RA4 pins, respectively.
DD0-DD7	It/Ot12	**Device Bus Data Line 0-7.** Connect to the MDP D0-D7 pins, respectively.
DRD#	Ot2	**Device Bus Read Enable.** Connect to the MDP READ# pin.
DWR#	Ot2	**Device Bus Write Enable.** Connect to the MDP WRITE# pin.
DRESET#	Ot2	**External Device Active Low Reset.** Connect to the MDP RESET1# and RESET2# pins.
WKRES#	Ot12	**Wakeup Reset.** Active low wake input. Connect to the MDP WKRES# pin.
MODEM_CS#	Ot2	**MDP Data Pump Chip Select.** MODEM_CS# output low selects the MDP. Connect to the MDP CS# pin.
MODEM_IRQ	It	**MDP Interrupt Request.** MODEM_IRQ is the active low interrupt request from the MDP. Connect to the MDP IRQ pin.
MODEM_CLK	Ot2	**Modem Clock.** Output clock for MDP. Connect to MDP XTLI pin.
M_TXCLK	It	**Modem Transmit Clock.** Connect to MDP M_TXCLK pin.
M_TX	Ot2	**Modem Transmit Data.** Connect to MDP M_TX pin.
M_RXCLK	It	**Modem Receive Clock.** Connect to MDP M_RXCLK pin.
M_RX	It	**Modem Receive Data.** Connect to MDP M_RX pin.
SI_FRAME	It/Ot	**SI Frame.** 8 kHz frame sync; rising edge starts frame. Connect to MDP SI_FRAME pin.
SI_CLK	It/Ot	**SI Clock.** Connect to MDP SI_CLK pin.
SI_DD	It	**SI Data Downstream.** Connect to MDP SI_DD pin.
SI_DU	Ot2	**SI Data Upstream.** Connect to MDP SI_DU pin.

Table 3-2. Bus Interface Pin Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
ISDN INTERFACE (NON-ISDN MODELS)		
DA0-DA3	Ot2	**Device Bus Address Lines 0-3.** Connect to the MDP only
DD0-DD7	It/Ot12	**Device Bus Data Line 0-7.** Connect to the MDP only
DRD#	Ot2	**Read Enable.** Connect to the MDP only
DWR#	Ot2	**Write Enable.** Connect to the MDP only
ISDN_CS#	Ot2	**ISDN Chip Select.** Leave open.
ISDN_INT	It	**ISDN Interrupt Request.** Connect to GND.
DRESET#	Ot2	**External Device Active Low Reset.** Leave open.
ISDN INTERFACE (ISDN MODELS)		
DA0-DA3	Ot2	**Device Bus Address Lines 0-3.** Connect to the ISDN interface device A0-A3 pins, respectively.
DD0-DD7	It/Ot12	**Device Bus Data Line 0-7.** Connect to the ISDN interface device D0-D7 pins, respectively.
DRD#	Ot2	**Read Enable.** Connect to the ISDN interface device RD# pin.
DWR#	Ot2	**Write Enable.** Connect to the ISDN interface device WR# pin.
ISDN_CS#	Ot2	**ISDN Chip Select.** Connect to the ISDN interface device CS# pin.
ISDN_INT	It	**ISDN Interrupt Request.** Connect to the ISDN interface device INT# pin.
DRESET#	Ot2	**External Device Active Low Reset.** Connect to the ISDN interface device RESET# pin.

Notes:

1. I/O types:

I/Opod	Input/Output, PCI, open drain (PCI type =o/d)
I/Opsts	Input/Output, PCI, sustained tristate (PCI type = s/t/s)
I/Opts	Input/Output, PCI, tristate (PCI type = t/s)
Ip	Input, PCI, totem pole (PCI type = in)
Ipts	Input, PCI (PCI type = t/s)
It	Input, TTL
It2	Input, TTL, 2 mA
Itpd	Input, TTL, internal pull-down
It/Ot	Input, TTL/Output, TTL
It/Ot12	Input, TTL/Output, TTL, 12 mA
Opod	Output, PCI, open drain (PCI type =o/d)
Opts	Output, PCI, tristate (PCI type = t/s)
Ot	Output, TTL
Ot2	Output, TTL, 2 mA
Ot4	Output, TTL, 4 mA
Ot12	Output, TTL, 12 mA

2. NC = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump

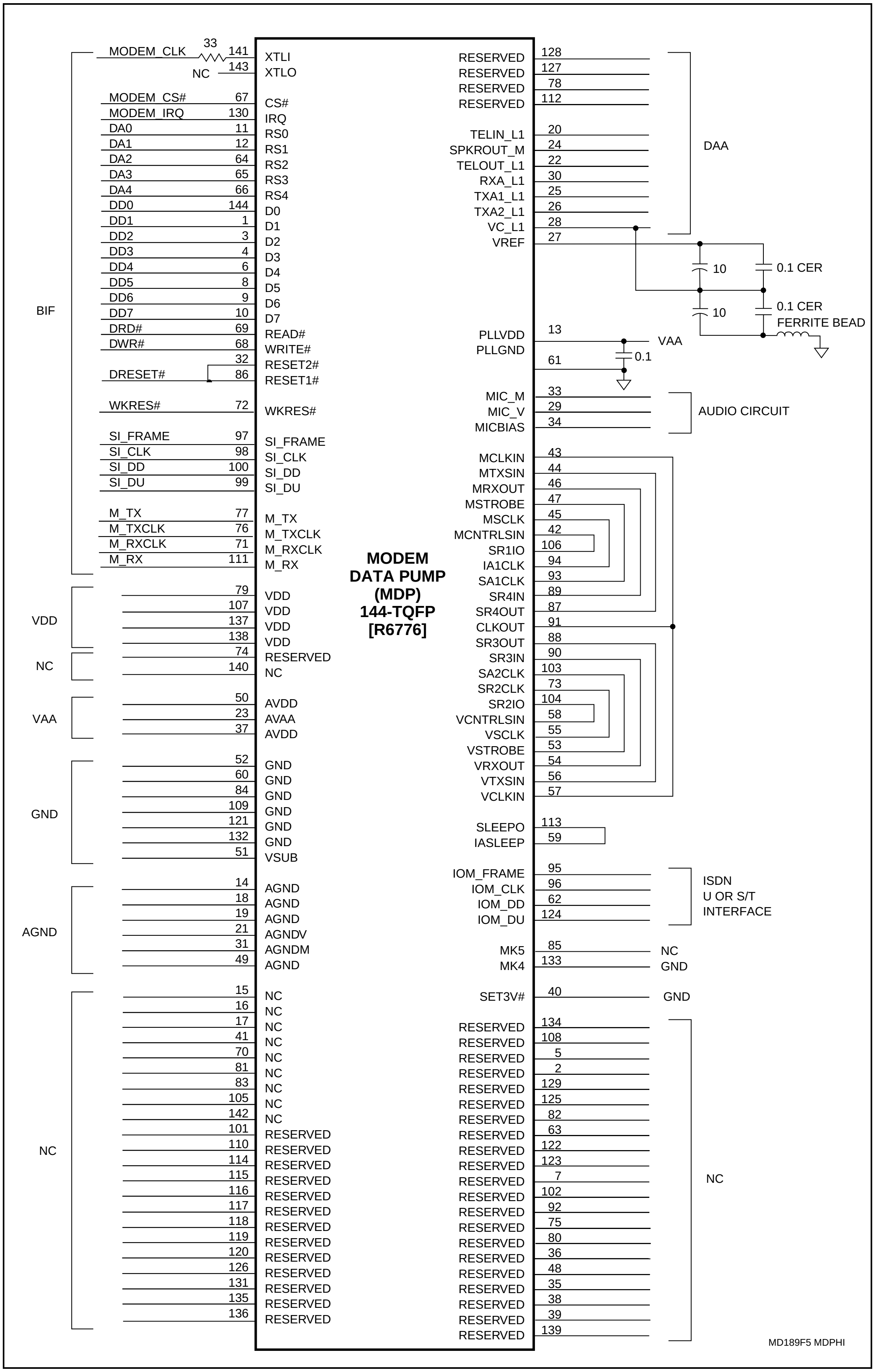


Figure 3-4. MDP 144-Pin TQFP Hardware Interface Signals

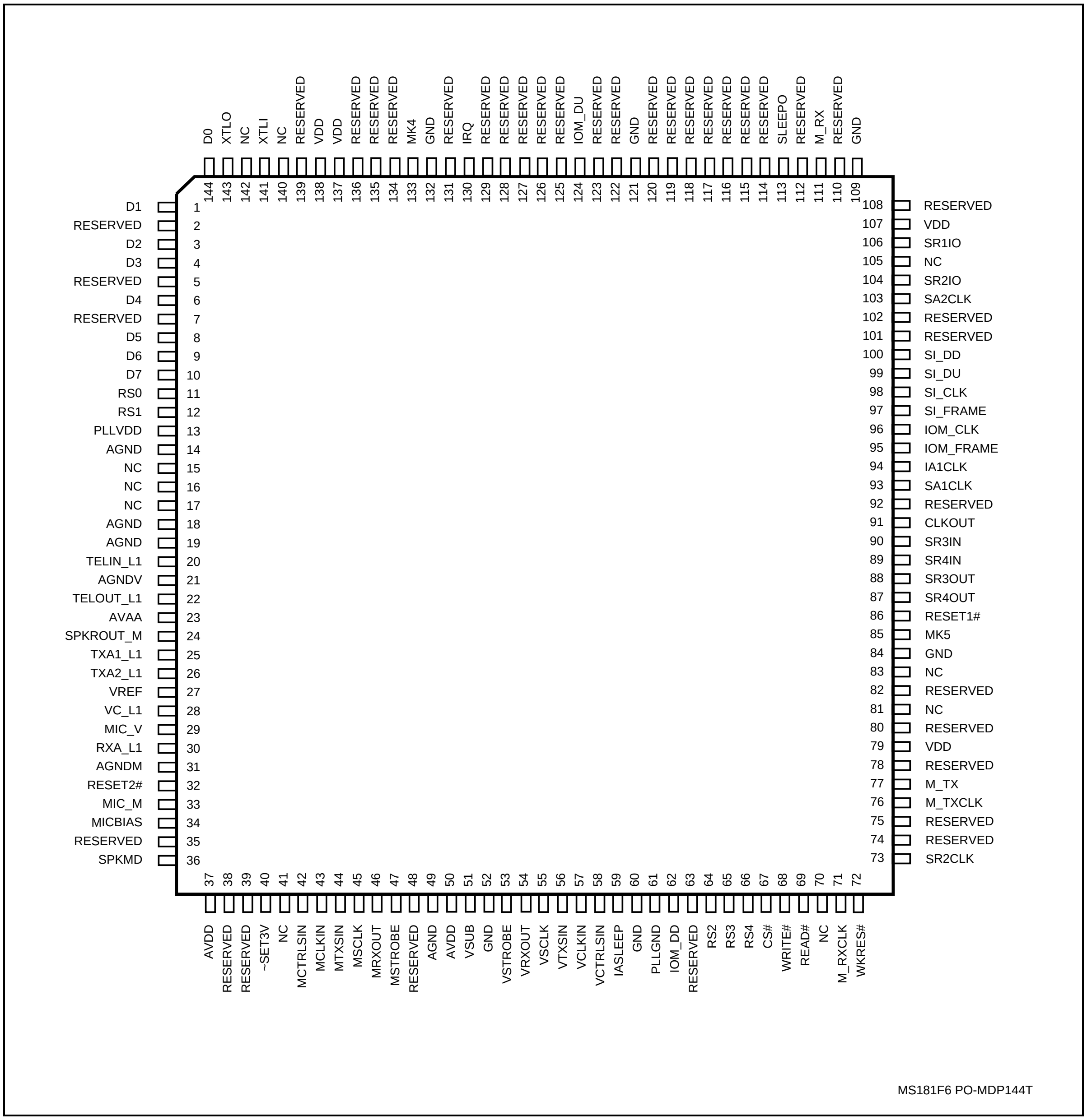


Figure 3-5. MDP 144-Pin TQFP Pin Signals

Table 3-3. MDP Pin Signals - 144-Pin TQFP

Pin	Signal Label	I/O Type[1]	Interface[3]	Pin	Signal Label	I/O Type[1]	Interface
1	D1	IA/OB	BIF: DD1	73	SR2CLK	DI	To VSCLK (55)
2	RESERVED		NC	74	RESERVED		NC
3	D2	IA/OB	BIF: DD2	75	RESERVED		NC
4	D3	IA/OB	BIF: DD3	76	M_TXCLK	OA	BIF: M_TXCLK
5	RESERVED		NC	77	M_TX	IA	BIF: M_TX
6	D4	IA/OB	BIF: DD4	78	RESERVED		NC
7	SYCLK	OA	Controller	79	VDD	PWR	VCC
8	D5	IA/OB	BIF: DD5	80	RESERVED		NC
9	D6	IA/OB	BIF: DD6	81	NC		NC
10	D7	IA/OB	BIF: DD7	82	RESERVED		NC
11	RS0	IA	BIF: DA0	83	NC		NC
12	RS1	IA	BIF: DA0	84	GND	GND	DGND
13	PLLVDD	PLL	To VAA and to AGND through 0.1 µF	85	MK5	IA	PLL Circuit Strap Option; NC
14	AGND	GND	AGND	86	RESET1#	IA	BIF: DRESET#
15	NC		NC	87	SR4OUT	DI	To MTXSIN (44)
16	NC		NC	88	SR3OUT	DI	To VTXSIN (56)
17	NC		NC	89	SR4IN	DI	To MRXOUT (46)
18	AGND	GND	AGND	90	SR3IN	DI	To VRXOUT (54)
19	AGND	GND	AGND	91	CLKOUT	DI	To MCLKIN (43) & VCLKIN (57)
20	TELIN_L1	I(DA)	DAA	92	RESERVED		NC
21	AGNDV	GND	AGND	93	SA1CLK	DI	To MSTROBE (47)
22	TELOUT_L1	O(DD)	DAA	94	IA1CLK	DI	To MSCLK (45)
23	AVAA	PWR	VAA	95	IOM_FRAME	IA/OB	ISDN: FSC
24	SPKROUT_M	O(DF)	Audio Circuit	96	IOM_CLK	IA/OB	ISDN: DCL
25	TXA1_L1	O(DD)	DAA	97	SI_FRAME	IA/OB	BIF: SI_FRAME
26	TXA2_L1	O(DD)	DAA	98	SI_CLK	IA/OB	BIF: SI_CLK
27	VREF	REF	VC_L1 through capacitors	99	SI_DU	IA	BIF: SI_DU
28	VC_L1	REF	AGND through capacitors	100	SI_DD	OA	BIF: SI_DD
29	MIC_V	I(DA)	Audio Circuit	101	RESERVED		NC
30	RXA_L1	I(DA)	DAA	102	RESERVED		NC
31	AGNDM	GND	AGND	103	SA2CLK	DI	To VSTROBE (53)
32	RESET2#	IA	BIF: DRESET#	104	SR2IO	DI	To VCNTRLSIN (58)
33	MIC_M	I(DA)	Audio Circuit	105	NC		NC
34	MICBIAS		Audio Circuit	106	SR1IO	DI	To MCNTRLSIN (42)
35	RESERVED		NC	107	VDD	PWR	VCC
36	SPKMD	OA	Sounducer	108	RESERVED		NC
37	AVDD	PWR	VCC	109	GND	GND	DGND
38	RESERVED		NC	110	RESERVED		NC
39	RESERVED		NC	111	M_RX	OA	BIF: M_RX
40	SET3V#	IA	To GND	112	RESERVED		NC
41	NC		NC	113	SLEEPO	DI	To IASLEEP (59)
42	MCNTRLSIN	DI	To SR1IO (106)	114	RESERVED		NC
43	MCLKIN	DI	To CLKOUT (91)	115	RESERVED		NC
44	MTXSIN	DI	To SR4OUT (87)	116	RESERVED		NC
45	MSCLK	DI	To IA1CLK (94)	117	RESERVED		NC
46	MRXOUT	DI	To SR4IN (89)	118	RESERVED		NC
47	MSTROBE	DI	To SA1CLK (93)	119	RESERVED		NC
48	RESERVED		NC	120	RESERVED		NC
49	AGND	GND	AGND	121	GND	GND	DGND
50	AVDD	PWR	VCC	122	YCLK	OA	NC
51	VSUB	GND	AGND	123	XCLK	OA	NC
52	GND	GND	DGND	124	IOM_DU	OA	ISDN: DIN
53	VSTROBE	DI	To SA2CLK (103)	125	RESERVED		NC
54	VRXOUT	DI	To SR3IN (90)	126	RESERVED		NC
55	VSCLK	DI	To SR2CLK (73)	127	RESERVED		NC
56	VTXSIN	DI	To SR3OUT (88)	128	RESERVED		NC
57	VCLKIN	DI	To CLKOUT (91)	129	RESERVED		NC
58	VCNTRLSIN	DI	To SR2IO (104)	130	IRQ	IA	BIF: MODEM_IRQ
59	IASLEEP	DI	To SLEEPO (113)	131	RESERVED		NC
60	GND	GND	DGND	132	GND	GND	DGND

Table 3-3. MDP Pin Signals - 144-Pin TQFP (Continued)

Pin	Signal Label	I/O Type[1]	Interface3	Pin	Signal Label	I/O Type[1]	Interface
61	PLLGND	PLL	To AGND	133	MK4	IA	PLL Circuit Strap Option; GND
62	IOM_DD	IA	ISDN: DOUT	136	RESERVED		NC
63	RESERVED		NC	135	RESERVED		NC
64	RS2	IA	BIF: DA02	136	RESERVED		NC
65	RS3	IA	BIF: DA03	137	VDD	PWR	VCC
66	RS4	IA	BIF: DA04	138	VDD	PWR	VCC
67	~CS	IA	BIF: MODEM_CS#	139	RESERVED		NC
68	DWR#	IA	BIF: DRD#	140	VTH2	IA	VDD through 10K Ω
69	DRD#	IA	BIF: DWR#	141	XTLI	I	BIF: L85CLK
70	NC		NC	142	NC		NC
71	M_RXCLK	OA	BIF: M_RXCLK	143	XTLO	O	NC
72	WKRES#	OA	BIF: WKRES#	144	D0	IA/OB	BIF: DD0

Notes:

1. I/O types:
   IA, IB = Digital input; OA, OB = Digital output (see Table 3-9).
   I(DA) = Analog input; O(DD), O(DF) = Analog output (see Table 3-10).
   DI = Device interconnect.
2. NC = No external connection allowed (may have internal connection).
3. Interface Legend:
   MDP = Modem Data Pump
   BIF = Bus Interface Device
   ISDN = ISDN U or S/T interface device.

Table 3-4. MDP Pin Signal Definitions

Label	I/O Type	Signal/Definition
OVERHEAD SIGNALS		
XTLI	I	**Crystal Int.** Connect the BIF MODEMCLK pin through a 33 Ω resistor.
XTLO	O	**Crystal Out.** Leave open.
VDD, AVDD	PWR	**Digital Power Supply.** To +3.3V and digital circuits power supply filter.
AVAA	PWR	**Analog Power Supply.** To +3.3V and analog circuits power supply filter.
GND	GND	**Digital Ground.** Connect to digital ground.
AGND	GND	**Analog Ground.** Connect to analog ground.
SET3V#	IA	**Set 3.3V Analog Reference.** Connect to digital ground.
BIF TO MDP INTERFACE		
RS0–RS4	IA	**Address Lines 0-4.** Connect to the BIF DA0–DA4 pins, respectively.
D0-D7	IA/OA	**Data Line 0-7.** Connect to the BIF DD0-DD7 pins, respectively.
READ#	IA	**Read Enable.** Connect to BIF DRD# pin.
WRITE#	IA	**Write Enable.** Connect to BIF DWR# pin.
RESET1#, RESET2#	IA	**External Device Active Low Reset.** Connect to the BIF DRESET# pin.
WKRES#	OA	**Wakeup Reset.** Active low wake-up output. Connect to the BIF WKRES# pin.
CS#	IA	**Chip Select.** CS# output low selects the MDP. Connect to the BIIF MODEM_CS# pin.
IRQ	OA	**Interrupt Request.** MODEM_IRQ is the active low interrupt request from the MDP. Connect to the BIF MODEM_IRQ pin.
M_TXCLK	OA	**Modem Transmit Clock.** Connect to BIF M_TXCLK pin.
M_TX	IA	**Modem Transmit Data.** Connect to BIF M_TX pin.
M_RXCLK	OA	**Modem Receive Clock.** Connect to BIF M_RXCLK pin.
M_RX	OA	**Modem Receive Data.** Connect to BIF M_RX pin.
SI_FRAME	IA/OB	**ISDN Frame.** 8 kHz frame sync; rising edge starts frame. Connect to BIF SI_FRAME pin.
SI_CLK	IA/OB	**ISDN Clock.** 1.536 MHz clock. Connect to BIF SI_CLK pin.
SI_DD	OA	**ISDN Data Downstream.** Connect to BIF SI_DD pin.
SI_DU	IA	**ISDN Data Upstream.** Connect to BIF SI_DU pin.
MDP TO SIEMENS PSB2186 S/T INTERFACE		
IOM_FRAME	IA/OB	**ISDN Frame Synchronization Clock.** 8 kHz frame sync; rising edge starts frame. The start of the B1 channel in time-slot 0 is marked. Connect to the ISDN device FSC pin.
IOM_CLK	IA/OB	**ISDN Clock.** 1.536 MHz clock. Connect to the ISDN device DCL pin.
IOM_DD	IA	**ISDN Data Downstream.** IOM data input synchronous to IOM_CLK. Connect to the ISDN device DOUT pin.
IOM_DU	OA	**ISDN Data Upstream.** IOM data output synchronous to IOM_CLK. Connect to the ISDN device DIN pin.
MDP TO SIEMENS PSB21910 U INTERFACE		
IOM_FRAME	IA/OB	**ISDN Frame Synchronization Clock.** 8 kHz frame sync; rising edge starts frame. The start of the B1 channel in time-slot 0 is marked. Connect to the ISDN device FSC pin.
IOM_CLK	IA/OB	**ISDN Clock.** 1.536 MHz clock. Connect to the ISDN device DCL pin.
IOM_DD	IA	**ISDN Data Downstream.** IOM data input synchronous to IOM_CLK. Connect to the ISDN device DOUT pin.
IOM_DU	OA	**ISDN Data Upstream.** IOM data output synchronous to IOM_CLK. Connect to the ISDN device DIN pin.

Table 3-4. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
TELEPHONE LINE/TELEPHONE/AUDIO INTERFACE SIGNALS AND REFERENCE VOLTAGE		
TXA1_L1 TXA2_L1	O(DF)	**Transmit Analog 1 and 2.** The TXA1_L1 and TXA2_L1 outputs are differential outputs 180 degrees out of phase with each other. Each output can drive a 300 Ω load.
RXA_L1	I(DA)	**Receive Analog.** RXA_L1 is a single-ended receive data input from the telephone line interface or an optional external hybrid circuit. The input impedance is > 70k Ω.
TELOUT_L1	O(DF)	**Telephone Handset Analog Output.** TELOUT_L1 is a single-ended analog output to the telephone handset speaker interface circuit. TELOUT_L1 can drive a 300 Ω load.
TELIN_L1	I(DA)	**Telephone Handset Analog Input.** TELIN_L1 is a single-ended analog input from the telephone handset microphone interface circuit. The input impedance is > 70k Ω.
MIC_M	I(DA)	**Modem Microphone Input.** MIC_M is a single-ended microphone input. The input impedance is > 70k Ω.
MIC_V	I(DA)	**Voice Microphone Input.** MIC_V is a single-ended microphone input. The input impedance is > 70k Ω.
SPKROUT_M	O(DF)	**Modem Speaker Analog Output.** The SPKROUT_M analog output reflects the received analog input signal. The SPKROUT_M on/off and three levels of attenuation are controlled by bits in DSP RAM. When the speaker is turned off, the SPKROUT_M output is clamped to the voltage at the VC_L1 pin. The SPKROUT_M output can drive an impedance as low as 300 ohms. In a typical application, the SPKROUT_M output is an input to an external LM386 audio power amplifier.
VREF	REF	**High Voltage Reference.** Connect to VC_L1 through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel.
VC_L1	REF	**Low Voltage Reference.** Connect to analog ground through 10 µF (polarized, + terminal to VC_L1) and 0.1 µF (ceramic) in parallel.
PLLVDD	PLL	**PLLVDD Connection.** Connect to VAA and to AGND through 0.1 µF.
PLLGND	PLL	**PLLGND Connection.** Connect to AGND.
MK4, MK5	IA	**PLL Circuit Strap Option.** Connect MK4 to digital ground and leave MK5 open in order to enable the internal PLL circuit.
SPKMD	OA	**Modem Speaker Digital Output.** The SPKMD digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator to create a PC Card (PCMCIA)-compatible signal.

Table 3-4. MDP Signal Definitions (Cont'd)

Label	I/O Type	Signal Name/Description
MODEM INTERCONNECT/NO CONNECT		
GPO0	DI	To M_RXCLK
SLEEPO	DI	To IASLEEP
IASLEEP	DI	To SLEEPO
MSCLK	DI	To IA1CLK
CLKOUT	DI	To MCLKIN & VCLKIN
SR1IO	DI	To MCTRLSIN
SR3IN	DI	To MRXOUT
IA1CLK	DI	To MSCLK
SA1CLK	DI	To MSTROBE
SR4OUT	DI	To MTXSIN
MCLKIN	DI	To CLKOUT
VCLKIN	DI	To CLKOUT
MSTROBE	DI	To SA1CLK
VSTROBE	DI	To SA2CLK
MCTRLSIN	DI	To SR1IO
VSCLK	DI	To SR2CLK
VCTRLSIN	DI	To SR2IO
MRXOUT	DI	To SR3IN
VTXSIN	DI	To SR3OUT
VRXOUT	DI	To SR4IN
MTXSIN	DI	To SR4OUT
SR2IO	DI	To VCTRLSIN
SR4IN	DI	To VRXOUT
SR2CLK	DI	To VSCLK
SA2CLK	DI	To VSTROBE
SR3OUT	DI	To VTXSIN
RESERVED		Reserved Function. May be connected to internal circuit. Leave open.

3.2 ELECTRICAL,SWITCHING,AND ENVIRONMENTAL CHARACTERISTICS

3.2.1 Power and Maximum Ratings

The current and power requirements are listed in Table 3-5.

The absolute maximum ratings are listed in Table 3-6.

Table 3-5. Current and Power Requirements

Mode	Current		Power		Notes
	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	
Bus Interface (11229)					f_{IN} = 28.224 MHz
Operating	145	186	479	670	
Modem Data Pump (R6776)					f_{IN} = 28.224 MHz
Operating	58	68	191	245	
Sleep	1.8	—	5.9	—	
Total					
MDP Operating	203	254	670	915	
MDP Sleep	147	—	485	—	

Notes:
Operating voltage: VDD = 3.3V ± 0.3V.
Test conditions: VDD = 3.3 VDC for typical values; VDD = 3.6 VDC for maximum values.

Table 3-6. Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Input Voltage	V_{IN}	-0.5 to (VCC +0.5)	V
Operating Temperature Range	T_A	-0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog Inputs	V_{IN}	-0.3 to (VAA+ 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	V_{HZ}	-0.5 to (VCC + 0.5)	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±400	mA

3.2.2 PCI Bus

Table 3-7 summarizes the PCI DC specifications for 3.3V signaling.

Table 3-8 summarizes the PCI AC specifications for 3.3V signaling.

Table 3-7. PCI Bus DC Specifications for 3.3V Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
Vcc	Supply Voltage		3.0	3.6	V	
Vih	Input High Voltage		0.5Vcc	Vcc +0.5	V	
Vil	Input Low Voltage		-0.5	0.3Vcc	V	
Vipu	Input Pull-up Voltage		0.7VCC		V	
Iil	Input Low Leakage Current	0<Vin <2Vcc		±10	µA	
Voh	Output High Voltage	Iout = -0.5 mA	0.9Vcc		V	
Vol	Output Low Voltage	Iout = 1.5 mA		0.1Vcc	V	
Cin	Input Pin Capacitance			10	pF	
Cclk	CLK Pin Capacitance		5	12	pF	
CIDSEL	IDSEL Pin Capacitance			8	pF	
Lpin	Pin Inductance			20	nH	

Table 3-8. PCI Bus AC Specifications for 3.3V Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
IOH(AC)	Switching Current High	0<Vout <0.3Vcc	-12Vcc		mA	
		0.3Vcc<Vout <0.9Vcc	-17.1(Vout -Vout)		mA	
		0.7Vcc<Vout <Vcc		Equation C		
	(Test Point)	Vout = 0.7Vcc		-32Vcc	mA	
IOL(AC)	Switching Current Low	Vout > Vout>0.6Vcc	16Vcc		mA	
		0.6Vcc>Vout> 0.1Vcc	Vout /0.023		mA	
		0.18Vcc>Vout >0		Equation D		
	(Test Point)	Vout = 0.18Vcc		38Vcc	mA	
Icl	Low Clamp Current	-3 < Vin ≤–1	-25+(Vin +1)/0.015		mA	
Ich	High Clamp Current	Vcc+4 > Vin > Vcc+1	25+(Vin -Vcc +1)/0.015		mA	
slew r	Output Rise Slew Rate	0.2Vcc - 0.6Vcc load	1	5	V / ns	
slew f	Output Fall Slew Rate	0.6Vcc - 0.2Vcc load	1	5	V / ns	

Notes:

Equation C: Ioh = (0.98/Vcc) * (Vout - Vcc) * (Vout + 0.4Vcc) for Vcc > Vout > 0.7Vcc.

Equation D: Iol = (256/Vcc) * Vout * (Vcc - Vout) for 0V < Vout < 0.18Vcc.

See PCI Bus Specification for complete details.

3.2.3 MDP

The MDP digital electrical characteristics for the hardware interface signals are listed in Table 3-9.

The MDP analog electrical characteristics for the hardware interface signals are listed in Table 3-10.

Table 3-9. MDP Digital Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions[1]
Input High Voltage	V_{IH}				VDC	
Type IA		2.0	–	VCC + 0.3		
Type IE		–	4.0	–		Note 2.
Input High Current	I_{IH}				µA	V_{IN}= 3.6 V, V_{CC} = 3.6 V
Type IB		–	–	40		
Input Low Voltage	V_{IL}				VDC	
Type IA		–0.3	–	0.8		
Type IE		–	1.0	–		Note 2.
Input Low Current	I_{IL}	–	–	-40	µA	
Input Leakage Current	I_{IN}			±2.5	µADC	V_{IN} = 0 to 3.3V, V_{CC} = 3.6 V
Output High Voltage	V_{OH}				VDC	
Type OA		2.4	–	–		I_{LOAD} = – 100 µA
Type OB		2.4	–	–		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				VDC	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Three-State (Off) Current	I_{TSI}			±10	µADC	V_{IN} = 0 V to VCC
Capacitive Load	C_L				pF	
Types IA and ID			–	10		
Type IB			–	20		
Capacitive Drive	C_D				pF	
Types OA and OB			–	10		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type ID						~RES
Types OA and OB						TTL with 3-state

Notes:

1. Test Conditions: VCC = 3.3V ±0.3V, TA = 0°C to 70°C, (unless otherwise stated).
   Output loads: Data bus (D0-D7), address bus (A0-A15), chip selects, DRD#, and DWR# loads = 70 pF + one TTL load.
   Other = 50 pF + one TTL load.
2. Type IE inputs are centered approximately 2.5 V and swing 1.5 V_{PEAK} in each direction.
3. Type OE outputs provide oscillator feedback when operating with an external crystal.

Table 3-10. Analog Electrical Characteristics

Name	Type	Characteristic	Value
RXA_L1, TELIN_L1	I (DA)	Input Impedance AC Input Voltage Range Reference Voltage	> 70K Ω 1.1 VP-P** +2.5 VDC
TXA1_L1 TXA2_L1 TELOUT_L1	O (DD)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0 µF 10 Ω 2.2 VP-P +2.5 VDC ± 200 mV
MIC_M MIC_V	I (DA)	Input Impedance Maximum AC Input Voltage Reference Voltage*	> 70K Ω 1.7 VP-P +2.5 VDC
SPKROUT_M	O (DF)	Minimum Load Maximum Capacitive Load Output Impedance AC Output Voltage Range Reference Voltage DC Offset Voltage	300 Ω 0.01 µF 10 Ω 1.1 VP-P +2.5 VDC ± 20 mV
* Reference Voltage provided internal to the device. ** Corresponds to 2.2 VP-P at Tip and Ring.			

3.3 INTERFACE TIMING AND WAVEFORMS

3.3.1 PCI Bus Timing

The PCI interface timing conforms to the PCI Local Bus Specification, Production Version, Revision 2.1, June 1, 1995.

3.3.2 Serial EEPROM Timing

The serial EEPROM interface timing is listed in Table 3-11 and is shown in Figure 3-6.

Table 3-11. Timing - Serial EEPROM Interface

Symbol	Parameter	Min	Typ.	Max	Units	Test Condition
t_{CSS}	Chip select setup	400	500	–	ns	
t_{CSH}	Chip select hold	400	500	–	ns	
t_{DOS}	Data output setup	400	500	–	ns	
t_{DOH}	Data output hold	400	500	–	ns	
t_{PD0}	Data input delay	–	–	400	ns	
t_{PD1}	Data input delay	–	–	400	ns	
t_{DF}	Data input disable time	–	–	100	ns	
t_{SV}	Status valid	–	–	100	ns	
t_{SKH}	Clock high	500	–	–	ns	
t_{SKL}	Clock low	500	–	–	ns	

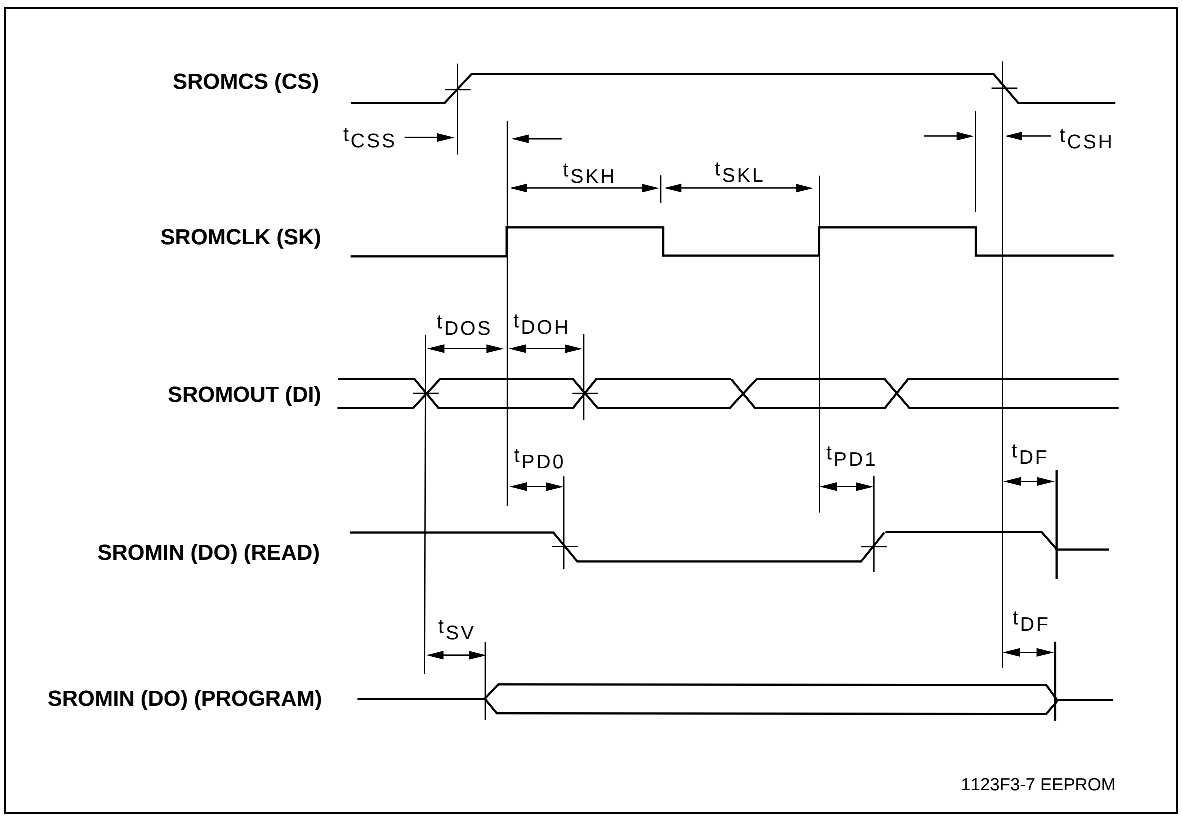


Figure 3-6. Waveforms - Serial EEPROM Interface

3.3.3 External Device Bus Timing

The external Device Bus timing is listed in Table 3-12 and illustrated in Figure 3-7.

Table 3-12. Timing - External Device Bus Interface

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions
Read						
t_{AS}	Address setup	40	–	–	ns	
t_{AH}	Address hold	10	–	–	ns	
t_{CSS}	Chip select setup	40	–	–	ns	
t_{CSH}	Chip select hold	108	–	144	ns	
t_{RW}	Read pulse width	150	–	–	ns	
t_{RDA}	Read data access	–	–	36	ns	
t_{RDH}	Read data hold	0	–	–	ns	
Write						
t_{AS}	Address setup	40	–	–	ns	
t_{AH}	Address hold	10	–	–	ns	
t_{CSS}	Chip select setup	40	–	–	ns	
t_{CSH}	Chip select hold	108	–	144	ns	
t_{WW}	Write pulse width	150	–	–	ns	
t_{WDS}	Write data setup	36	–	–	ns	
t_{RDH}	Write data hold	36	–	72	ns	

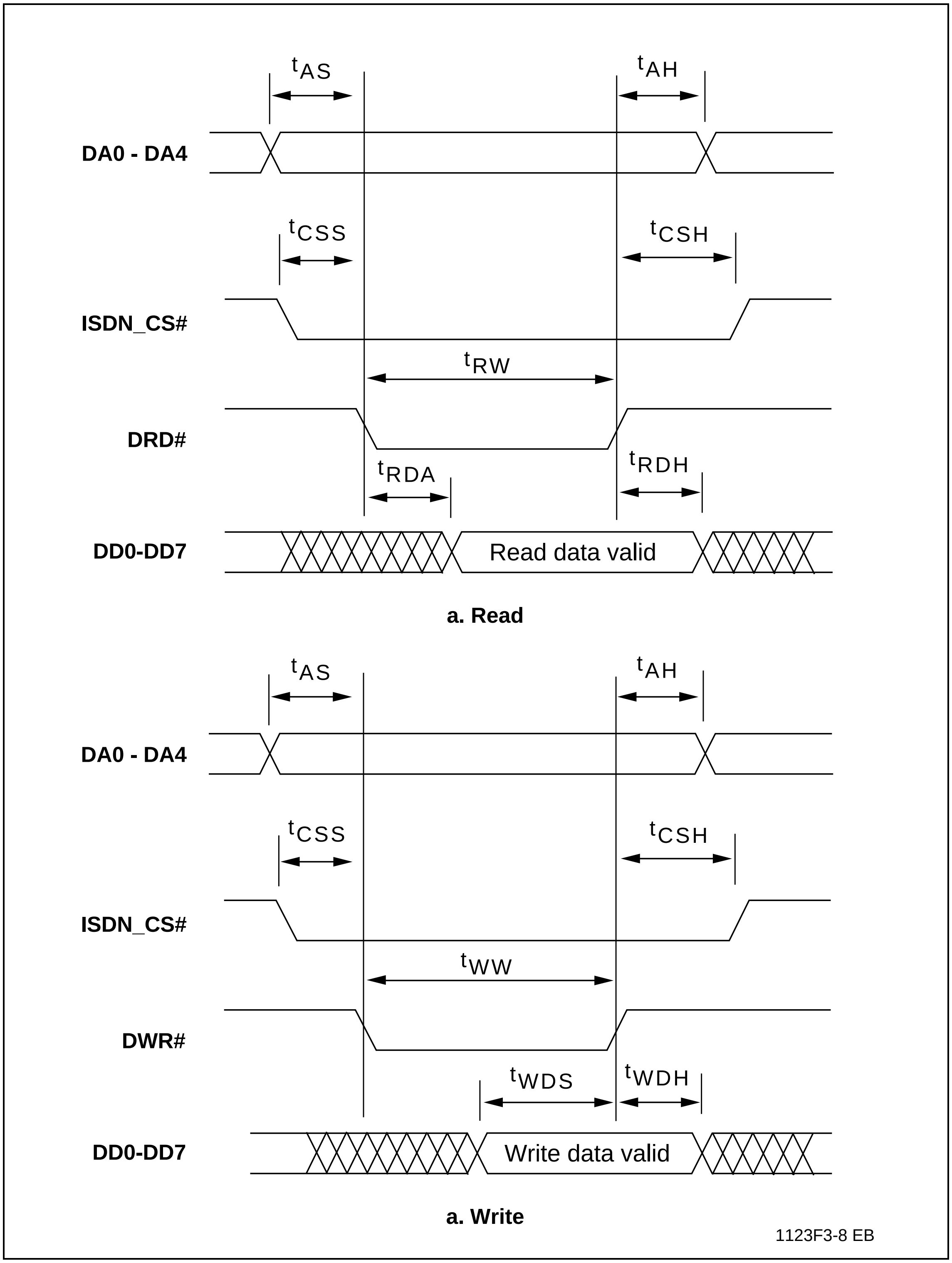


Figure 3-7. Waveforms - External Device Bus Interface

3.3.4 IOM-2 Interface

The interface timing is listed in Table 3-13 and shown in Figure 3-8.

Table 3-13. Timing - IOM-2 Interface

Symbol	Parameter	Min	Typ.	Max	Units	Test Condition
t_r, t_f	Data clock (DCL) and frame sync (FSC) rise/fall	–	–	30	ns	C_L = 25 pF
t_{DCL}	Data clock period (note 1)	565	651	735	ns	C_L = 25 pF
t_{wH}, t_{wL}	Data clock pulse width high/low (note 1)	200	310	420	ns	
t_{sD}	Data setup	32	–	–	ns	
t_{hD}	Data hold	32	–	–	ns	
t_{dF}	Frame advance	0	65	130	ns	C_L = 25 pF
t_{hF}	Frame hold	20	–	–	ns	C_L = 25 pF
t_{dDC}	Data delay clock	–	20	100	ns	C_L = 150 pF
t_{dDF}	Data delay frame	–	–	150	ns	C_L = 150 pF

Notes:
1. 768 bps.

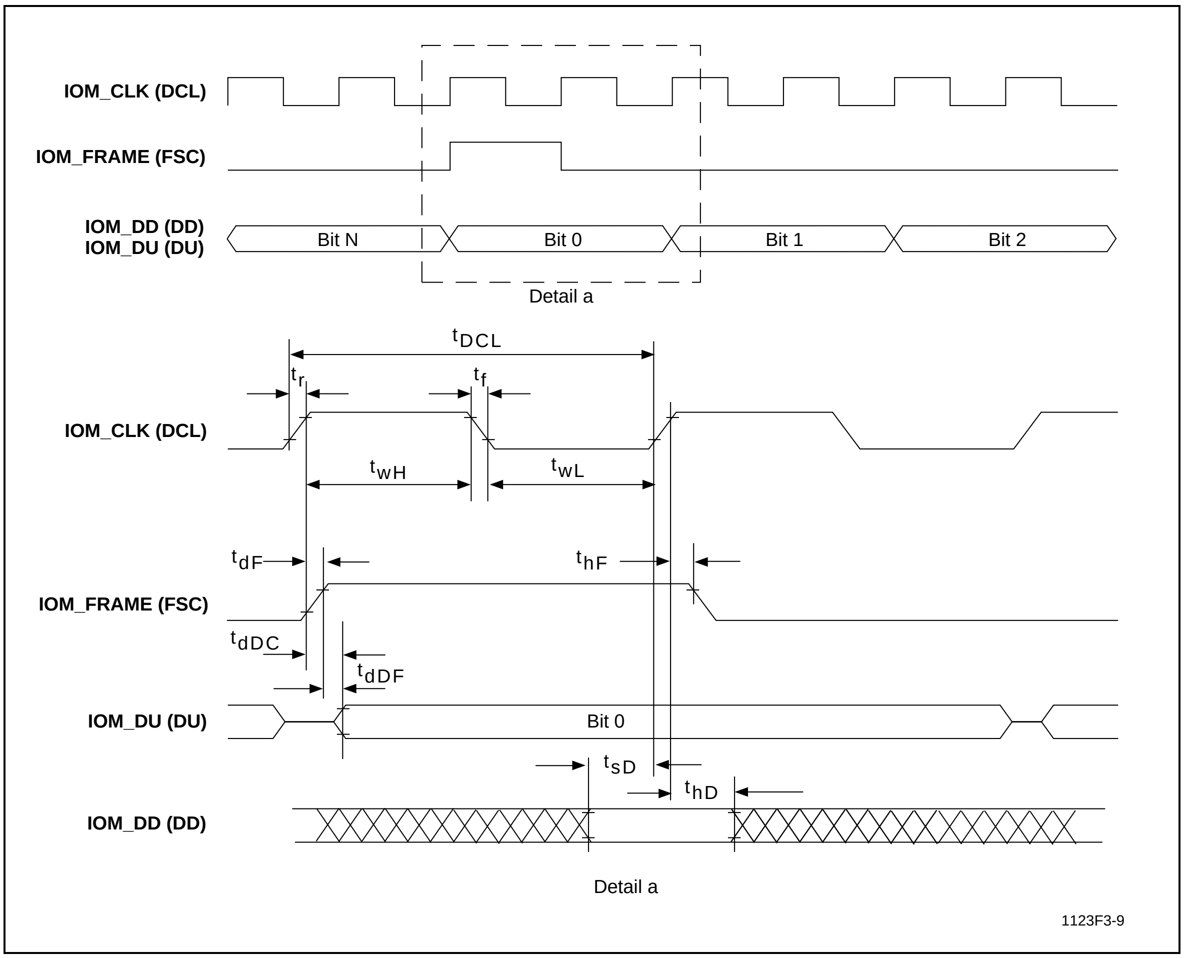


Figure 3-8. Waveforms - IOM-2 Interface

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4. DESIGN CONSIDERATIONS

Good engineering practices must be followed when designing a printed circuit board (PCB) containing the modem device. This is especially important considering the high data bit rate, high fax rate, record/play of analog speech and music audio, and full-duplex speakerphone operation. Suppression of noise is essential to the proper operation and performance of the modem and interfacing audio and DAA circuits.

Two aspects of noise in an OEM board design containing the modem device set must be considered: on-board/off-board generated noise that can affect analog signal levels and analog-to-digital conversion (ADC)/digital-to-analog conversion (DAC), and on-board generated noise that can radiate off-board. Both on-board and off-board generated noise that is coupled on-board can affect interfacing signal levels and quality, especially in low level analog signals. Of particular concern is noise in frequency ranges affecting modem and audio circuit performance.

On-board generated electromagnetic interference (EMI) noise that can be radiated or conducted off-board is a separate, but equally important, concern. This noise can affect the operation of surrounding equipment. Most local governing agencies have stringent certification requirements that must be met for use in specific environments. In order to minimize the contribution of the circuit design and PCB layout to EMI, the designer must understand the major sources of EMI and how to reduce them to acceptable levels.

Proper PC board layout (component placement and orientation, signal routing, trace thickness and geometry, etc.), component selection (composition, value, and tolerance), interface connections, and shielding are required for the board design to achieve desired modem performance and to attain EMI certification. In addition, design layout should meet requirements stated in the PCI Bus Specification, Section 4.4, Expansion Board Specification, as well as other applicable sections.

All the aspects of proper engineering practices are beyond the scope of this designer's guide. The designer should consult noise suppression techniques described in technical publications and journals, electronics and electrical engineering text books, and component supplier application notes. Seminars addressing noise suppression techniques are often offered by technical and professional associations as well as component suppliers.

The following guidelines are offered to specifically help achieve stated modem performance, minimize audible noise for audio circuit use, and to minimize EMI generation.

4.1 PC BOARD LAYOUT GUIDELINES

4.1.1 General Principles

1. Provide separate digital, analog, and DAA sections on the board.
2. Keep digital and analog components and their corresponding traces as separate as possible and confined to defined sections.
3. Keep high speed digital traces as short as possible.
4. Keep sensitive analog traces as short as possible.
5. Provide proper power supply distribution, grounding, and decoupling.
6. Provide separate digital ground, analog ground, and chassis ground (if appropriate) planes.
7. Provide wide traces for power and critical signals.
8. Position digital circuits near the host bus connection and position the DAA circuits near the telephone line connections.

4.1.2 Component Placement

1. From the system circuit schematic,
   a) Identify the digital, analog, and DAA circuits and their components, as well as external signal and power connections.
   b) Identify the digital, analog, mixed digital/analog components within their respective circuits.
   c) Note the location of power and signals pins for each device (IC).
2. Roughly position digital, analog, and DAA circuits on separate sections of the board. Keep the digital and analog components and their corresponding traces as separate as possible and confined to their respective sections on the board. Typically, the digital circuits will cover one-half of the board, analog circuits will cover one-fourth of the board, and the DAA will cover one-fourth of the board. **NOTE:** While the DAA is primarily analog in nature, it also has many control and status signals routed through it. A DAA section is also governed by local government regulations covering subjects such as component spacing, high voltage suppression, and current limiting.

3. Once sections have been roughly defined, place the components starting with the connectors and jacks.
   a) Allow sufficient clearance around connectors and jacks for mating connectors and plugs.
   b) Allow sufficient clearance around components for power and ground traces.
   c) Allow sufficient clearance around sockets to allow the use of component extractors.
4. First, place the mixed analog/digital components (e.g., modem device, A/D converter, and D/A converter).
   a) Orient the components so pins carrying digital signals extend onto the digital section and pins carrying analog signals extend onto the analog section as much as possible.
   b) Position the components to straddle the border between analog and digital sections.
5. Place all analog components.
   a) Place the analog circuitry, including the DAA, on the same area of the PCB.
   b) Place the analog components close to and on the side of board containing the TXA1_L1, TXA2_L1, RXA_L1, VC_L1, and VREF signals.
   c) Avoid placing noisy components and traces near TXA1_L1, TXA2_L1, RXA_L1, VC_L1, and VREF lines.
6. Place active digital components/circuits and decoupling capacitors.
   a) Place digital components close together in order to minimize signal trace length.
   b) Place 0.1 µF decoupling (bypass) capacitors close to the pins (usually power and ground) of the IC they are decoupling. Make the smallest loop area possible between the capacitor and power/ground pins to reduce EMI.
   c) Place host bus interface components close to the edge connector in accordance with the applicable bus interface standard, e.g., the PCI Bus Specification.
   d) Place crystal circuits as close as possible to the devices they drive.
7. Provide a “connector” component, usually a zero ohm resistor or a ferrite bead at one or more points on the PCB to connect one section’s ground to another.

4.1.3 Signal Routing

1. Route the modem signals to provide maximum isolation between noise sources and noise sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. The noise source, neutral, and noise sensitive pins are listed in Table 4-1.
2. Keep digital signals within the digital section and analog signals within the analog section. (Previous placement of isolation traces should prevent these traces from straying outside their respective sections.) Route the digital traces perpendicular to the analog traces to minimize signal cross coupling.
3. Provide isolation traces (usually ground traces) to ensure that analog signals are confined to the analog section and digital traces remain out of the analog section. A trace may have to be narrowed to route it though a mixed analog/digital IC, but try to keep the trace continuous.
   a) Route an analog isolation ground trace, at least 50 mil to 100 mil wide, around the border of the analog section; put on both sides of the PCB.
   b) Route a digital isolation ground trace, at least 50 mil to 100 mil wide, and 200 mil wide on one side of the PCB edge, around the border of the digital section.
4. Keep host interface signals (e.g., AEN, IOR#, IOW#, HRESET) traces at least 10 mil thick (preferably 12 - 15 mil).
5. Keep analog signal (e.g., the TXA1_L1, TXA2_L1, RXA_L1, TELIN_L1, TELOUT_L1 , MIC_M, MIC_V, and SPKROUT_M) traces at least 10 mil thick (preferably 12 - 15 mil).
6. Keep all other signal traces as wide as possible, at least 5 mil (preferably 10 mil).Route the signals between components by the shortest possible path (the components should have been previously placed to allow this).
7. Route the traces between bypass capacitors to IC pins, at least 25 mil wide; avoid vias if possible.
8. Gather signals that pass between sections (typically low speed control and status signals) together and route them between sections through a path in the isolation ground traces at one (preferred) or two points only. If the path is made on one side only, then the isolation trace can be kept contiguous by briefly passing it to the other side of the PCB to jump over the signal traces.
9. Avoid right angle (90 degree) turns on high frequency traces. Use smoothed radiuses or 45 degree corners.

10. Minimize the number of through-hole connections (feedthroughs/vias) on traces carrying high frequency signals.
11. Keep all signal traces away from crystal circuits.
12. Distribute high frequency signals continuously on a single trace rather than several traces radiating from one point.
13. Provide adequate clearance (e.g., 60 mil minimum) around feedthroughs in any internal planes in the DAA circuit.
14. Eliminate ground loops, which are unexpected current return paths to the power source.

4.1.4 Power

1. Identify digital power (VDD) and analog power (AVDD) supply connections.
2. Place a 10 µF electrolytic or tantalum capacitor in parallel with a ceramic 0.1 µF capacitor between power and ground at one or more points in the digital section. Place one set nearest to where power enters the PCB (edge connector or power connector) and place another set at the furthest distance from where power enters the PCB. These capacitors help to supply current surge demands by the digital circuits and prevent those surges from generating noise on the power lines that may affect other circuits.
3. For 2-layer boards, route a 200-mil wide power trace on two edges of the same side of the PCB around the border of the circuits using the power. (Note that a digital ground trace should likewise be routed on the other side of the board.)
4. Generally, route all power traces before signal traces.

Table 4-1. Modem Pin Noise Characteristics

Device	Function	Noise Source	Neutral	Noise Sensitive
MDP	VDD, VAA		13, 27, 40, 49, 63, 85-86	
144-Pin TQFP	GND, DGND, AGND		16, 39, 48, 81, 99	
	Crystal	87-88		
	Control		17, 35, 56, 68	
	Line Interface		31-32, 37, 47, 78	25-26, 29-30, 33-34, 36
	Speaker Interface		38	28
	Serial/LED Interface	7, 10-11, 64, 66, 82	9, 12, 67, 75, 77, 79	
	Host Interface	1-6, 89-98	80	
	MDP Interconnect	8, 18-24, 41-46, 50-55, 59-60, 62		
	Reserved or NC		14-15, 57-58, 61, 65, 69-74, 76, 83-84, 100	

4.1.5 Ground Planes

1. In a 2-layer design, provide digital and analog ground plane areas in all unused space around and under digital and analog circuit components (exclusive of the DAA), respective, on both sides of the board, and connect them such a manner as to avoid small islands. Connect each ground plane area to like ground plane areas on the same side at several points and to like ground plane areas on the opposite side through the board at several points. Connect all modem DGND pins to the digital ground plane area and AGND pins to the analog ground plane area. Typically, separate the collective digital ground plane area from the collective analog ground plane area by a fairly straight gap. There should be no inroads of digital ground plane area extending into the analog ground plane area or visa versa.
2. In a 4-layer design, provide separate digital and analog ground planes covering the corresponding digital and analog circuits (exclusive of the DAA), respectively. Connect all modem DGND pins to the digital ground plane and AGND pins to the analog ground plane. Typically, separate the digital ground plane from the analog ground plane by a fairly straight gap.
3. In a design which needs EMI filtering, define an additional "chassis" section adjacent to the bracket end of a plug-in card. Most EMI components (usually ferrite beads/capacitor combinations) can be positioned in this section. Fill the unused space with a chassis ground plane, and connect it to the metal card bracket and any connector shields/grounds.
4. Keep the current paths of separate board functions isolated, thereby reducing the current's travel distance. Separate board functions are: host interface, display, digital (SRAM, EPROM, modem), and DAA. Power and ground for each of these functions should be separate islands connected together at the power and ground source points only.
5. Connect grounds together at only one point, if possible, using a ferrite bead. Allow other points for grounds to be connected together if necessary for EMI suppression.
6. Keep all ground traces as wide as possible, at least 25 mil to 50 mil.
7. Keep the traces connecting all decoupling capacitors to power and ground at their respective ICs as short and as direct (i.e., not going through vias) as possible.

4.1.6 Crystal Circuit

1. Keep all traces and component leads connected to crystal input and output pins (i.e., XTLI and XTLO) short in order to reduce induced noise levels and minimize any stray capacitance that could affect the crystal oscillator. Keep the XTLO trace extremely short with no bends greater than 45 degrees and containing no vias since the XTLO pin is connected to a fast rise time, high current driver.
2. Where a ground plane is not available, such as in a 2-layer design, tie the crystal capacitors ground paths using separate short traces (as wide as possible) with minimum angles and vias directly to the corresponding device digital ground pin nearest the crystal pins.
3. Connect crystal cases(s) to ground (if applicable).
4. Place a 100-ohm (typical) resistor between the XTLO pin and the crystal/capacitor node.
5. Connect crystal capacitor ground connections directly to GND pin on the modem device. Do not use common ground plane or ground trace to route the capacitor GND pin to the corresponding modem GND pin.

4.1.7 VC_L1 and VREF Circuit

1. Provide extremely short, independent paths for VC_L1 and VREF capacitor connections.
   a) Route the connection from the plus terminal of the 10 µF VC_L1 capacitor and one terminal of the 0.1 µF VC_L1 capacitor to the modem device VC_L1 pin (pin 24) using a single trace isolated from the trace to the VC_L1 pin from the VREF capacitors (see step d).
   b) Route the connection from the negative terminal of the 10 µF VC_L1 capacitor and the other terminal of a the 0.1 µF VC_L1 capacitor to a ferrite bead. The bead should typically have characteristics such as: impedance = 70 Ω at a frequency of 100 MHz , rated current = 200 mA, and maximum resistance = 0.5 Ω. Connect the other bead terminal to the AGND pin (pin 34) with a single trace.
   c) Route the connection from the plus terminal of the 10 µF VREF capacitor and one terminal of the 0.1 µF VREF capacitor to the modem device VREF pin (pin 25) with a single trace.
   d) Route the connection from the negative terminal of 10 µF VREF capacitor and the other terminal of the 0.1 µF VREF capacitor to the modem device VC_L1 pin (pin 24) with a single trace isolated from the trace to the VC_L1 pin from the VC_L1 capacitors (see step a).

4.1.8 Telephone and Local Handset Interface

1. Place common mode chokes in series with Tip and Ring for each connector.
2. Decouple the telephone line cables at the telephone line jacks. Typically, use a combination of series inductors, common mode chokes, and shunt capacitors. Methods to decouple telephone lines are similar to decoupling power lines, however, telephone line decoupling may be more difficult and deserves additional attention. A commonly used design aid is to place footprints for these components and populate as necessary during performance/EMI testing and certification.
3. Place high voltage filter capacitors (.001 µF @1KV) from Tip and Ring to digital ground.

4.1.9 Optional Configurations

Because fixed requirements of a design may alter EMI performance, guidelines that work in one case may deliver little or no performance enhancement in another. Initial board design should, therefore, include flexibility to allow evaluation of optional configurations. These optional configurations may include:

1. Chokes in Tip and Ring lines replaced with jumper wires as a cost reduction if the design has sufficient EMI margin.
2. Various grounding areas connected by tie points (these tie points can be short jumper wires, solder bridges between close traces, etc.).
3. Develop two designs in parallel; one based on a 2-layer board and the other based on a 4-layer board. During the evaluation phase, better performance of one design over another may result in quicker time to market.

4.1.10 MDP Specific

1. Locate the MDP device and all supporting analog circuitry, including the data access arrangement, on the same area of the PCB.
2. Locate the analog components close to and on the side of board containing the TXA1_L1, TXA2_L1, RXA_L1, TELIN_L1, TELOUT_L1 , MIC_M, MIC_V, and SPKROUT_M signals.
3. Avoid placing noisy components and traces near the TXA1_L1, TXA2_L1, RXA_L1, TELIN_L1, TELOUT_L1 , MIC_M, MIC_V, and SPKROUT_M lines.
4. Route MDP modem interconnect signals by the shortest possible route avoiding all analog components.
5. Provide an RC network on the AVAA supply in the immediate proximity of the AVAA pin to filter out high frequency noise above 115 kHz. A tantalum capacitor is recommended (especially in a 2-layer board design) for improved noise immunity with a current limiting series resistor or inductor to the VCC supply which meets the RC filter frequency requirements.
6. Provide a 0.1 µF ceramic decoupling capacitor to ground between the high frequency filter and the VAA pin.
7. Provide a 0.1 µF ceramic decoupling capacitor to ground between the VCC supply and the AVDD pin.

4.2 CRYSTAL/OSCILLATOR SPECIFICATIONS

Recommended surface-mount crystal specifications are listed in Table 4-2.

Recommended through-hole crystal specifications are listed in Table 4-3.

4.3 OTHER CONSIDERATIONS

The DAA design described in this designer's guide is a wet DAA, i.e., it requires line current to be present to pass the signal. Therefore, if the modem is to be connected back-to-back by cable directly to another modem, the modems will not be able to connect. The DAAs must be modified to operate dry, i.e., without line current, when used in this environment.

A complete schematic is available for the RCV56HCF Data/Fax Modem PCI Half Card Reference Design (TR04-D380).

Table 4-2. Crystal Specifications - Surface Mount

Characteristic	Value
Rockwell Part No.	5333R02-020
Electrical	
Frequency	28.224 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability	
vs. Temperature	±35 ppm (0°C to 70°C)
vs. Aging	±15 ppm/4 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	60 Ω max. @20 nW drive level
Drive Level	100µW correlation; 300µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions (L x W x H)	7.5 x 5.2 x 1.3 mm max.
Mounting	SMT
Holder Type	None
Suggested Suppliers	
	KDS America
	ILSI America
	Vectron Technologies, Inc.

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

KDS America
Fountain Valley, CA 92626
(714) 557-7833

ILSI America
Kirkland, WA 98033
(206) 828 - 4886

Vectron Technologies, Inc.
Lowell, NH 03051
(603) 598-0074

Toyocom U.S.A., Inc.
Costa Mesa, CA
(714) 668-9081

Table 4-3. Crystal Specifications - Through Hole

Characteristic	Value
Rockwell Part No.	333R44-011
Electrical	
Frequency	28.224 MHz nom.
Frequency Tolerance	±50 ppm (C_L = 16.5 and 19.5 pF)
Frequency Stability	
vs. Temperature	±30 ppm (0°C to 70°C)
vs. Aging	±20 ppm/5 years
Oscillation Mode	Fundamental
Calibration Mode	Parallel resonant
Load Capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series Resistance, R_1	35 Ω max. @20 nW drive level
Drive Level	100µW correlation; 500µW max.
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to 85°C
Mechanical	
Dimensions (L x W x H)	11.05 x 4.65 x 13.46 mm max.
Mounting	Through Hole
Holder Type	HC-49/U
Suggested Suppliers	KDS America ILSI America Vectron Technologies, Inc.

Notes

1. Characteristics @ 25°C unless otherwise noted.
2. Supplier Information:

   KDS America
   Fountain Valley, CA 92626
   (714) 557-7833

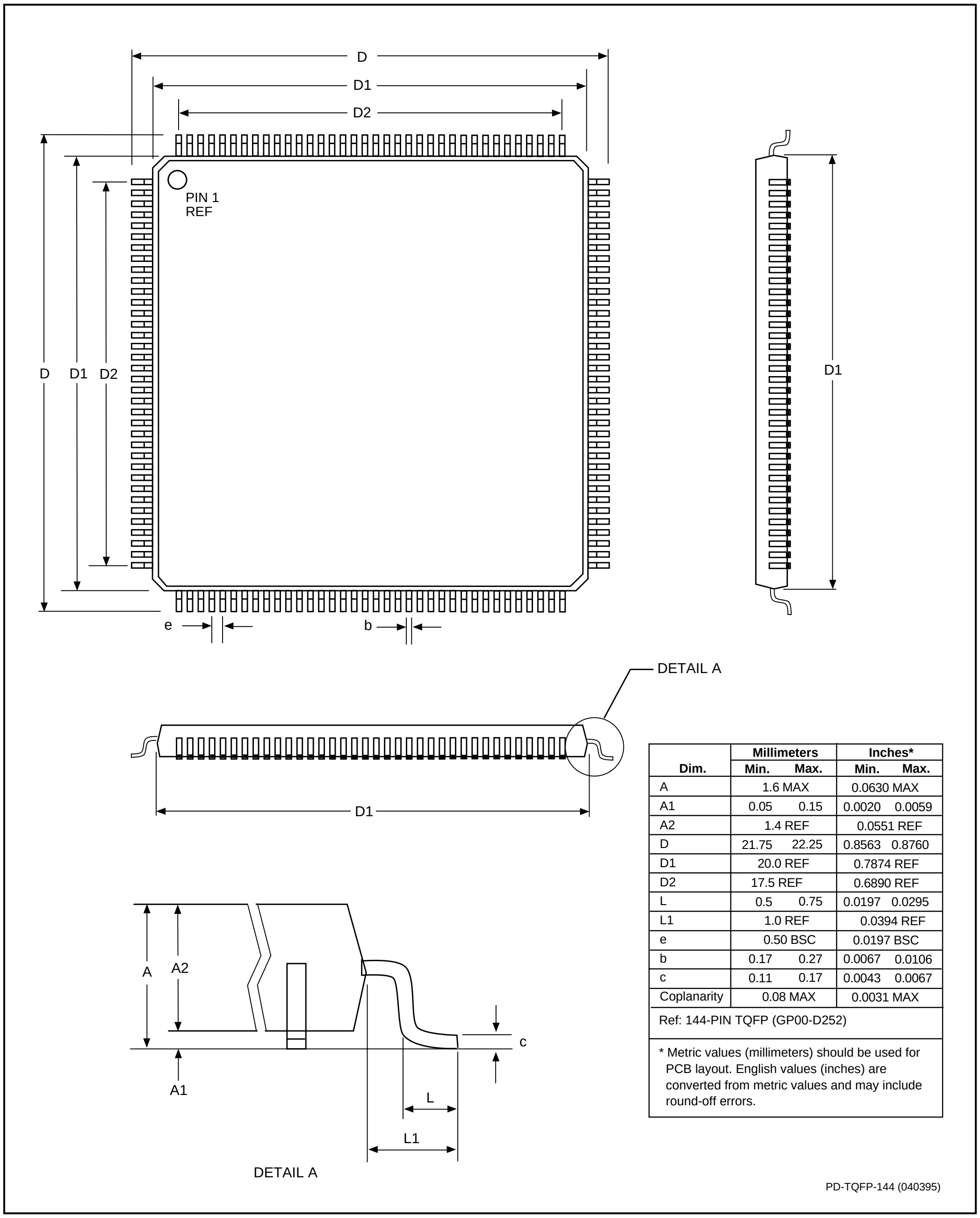
   ILSI America
   Kirkland, WA 98033
   (206) 828 - 4886

   Vectron Technologies, Inc.
   Lowell, NH 03051
   (603) 598-0074

   Toyocom U.S.A., Inc.
   Costa Mesa, CA
   (714) 668-9081

4.4 PACKAGE DIMENSIONS

The package dimensions are shown in Figure 4-1 (144-pin TQFP) and Figure 4-2 (176-pin TQFP) .



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	17.5 REF		0.6890 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

Ref: 144-PIN TQFP (GP00-D252)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

Figure 4-1. Package Dimensions - 144-Pin TQFP

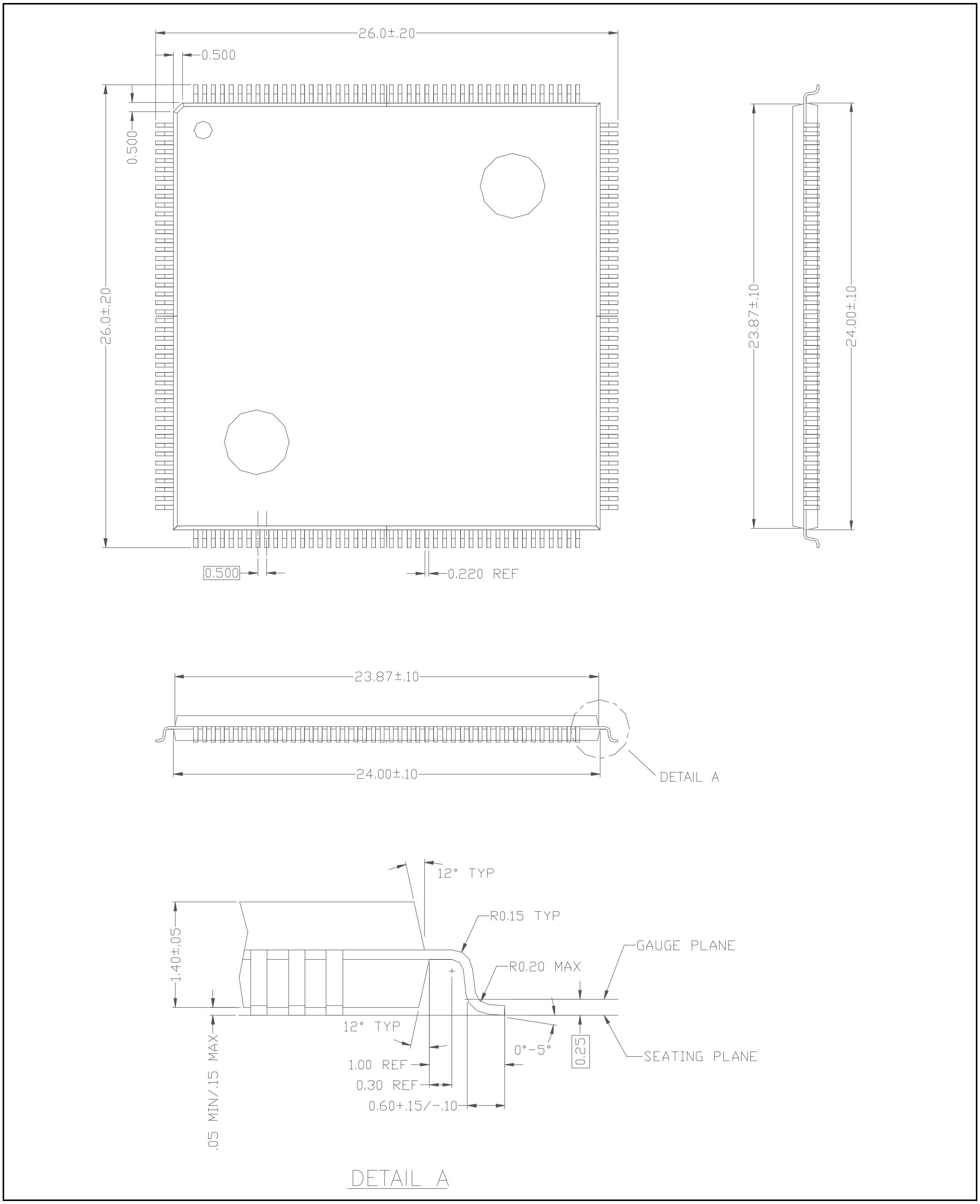


Figure 4-2. Package Dimensions - 176-Pin TQFP

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5. SOFTWARE INTERFACE

5.1 PCI Configuration Registers

The PCI Configuration registers are located in the BIF. Table 5-1 identifies the configuration register contents that are supported in the BIF device:

Table 5-1. PCI Configuration Registers

Offset (Hex)	Bit			
	31:24	23:16	15:8	7:0
0	Device ID		Vendor ID	
4	Status		Command	
8	Class Code			Revision ID
C	Not Implemented	Header Type	Latency Timer	Not Implemented
10	Base Address 0 - Memory (BIF)			
14	Unused Base Address Register			
18	Unused Base Address Register			
1C	Unused Base Address Register			
20	Unused Base Address Register			
24	Unused Base Address Register			
28	CIS Pointer			
2C	Subsystem ID		Subsystem Vendor ID	
30	Not Implemented			
34	Reserved			
38	Reserved			
3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line

5.1.1 Vendor ID Field

This field is read-only and is loaded from the serial EEPROM after reset events. The default value for the Vendor ID is 127a.

5.1.2 Device ID Field

This field is read-only and is loaded from the serial EEPROM after reset events.

5.1.3 Command Register

The Command Register bits are described in Table 5-2.

Table 5-2. Command Register

Bit	Description
0	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.
1	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0.
2	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. State after RST# is 0.
3	Not Implemented.
4	Not Implemented.
5	Not Implemented.
6	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device must ignore any parity errors that it detects and continue normal operation. This bit's state after RST# is 0.
7	This bit is used to control whether or not a device does address/data stepping. This bit is read only from the PCI interface. It is loaded from the serial EEPROM after RST#.
8	This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver. This bit's state after RST# is 0.
9	This bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 1 means the master is allowed to generate fast back-to-back transactions to different agents as described in Section 3.4.2 of the PCI 2.1 specification. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
10-15	Reserved

5.1.4 Status Register

The Status Register bits are described in Table 5-3.

Status register bits may be cleared by writing a '1' in the bit position corresponding to the bit position to be cleared. It is not possible to set a status register bit by writing from the PCI Bus. Writing a '0' has no effect in any bit position.

Table 5-3. Status Register

Bit	Description
0-4	Reserved
5	Not Implemented.
6	Not Implemented.
7	Not Implemented.
8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command Register) is set.
9-10	These bits encode the timing of DEVSEL#. These are encoded as 00 for fast, 01 for medium, and 10 for slow (11 is reserved.) These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
11	Not Implemented.
12	This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
13	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
14	This bit must be set whenever the device asserts SERR#. Devices which will never assert SERR# do not need to implement this bit.
15	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

5.1.5 Revision ID Field

Initial part hardwired to 00.

5.1.6 Class Code Field

Hardwired to 0x078000 to indicate communications controller.

5.1.7 Latency Timer Register

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. This register has 5 read/write bits (MSBs) plus 3 bits of hardwired zero (LSBs). The Latency Timer Register is loaded into the PCI Latency counter each time FRAME# is asserted to determine how long the master is allowed to retain control of the PCI bus. This register is loaded by system software. The default value for Latency Timer is 00.

5.1.8 Header Type Field

Hardwired to 00.

5.1.9 CIS Pointer Register

This register points to the CIS memory located in the BIF's memory space.

5.1.10 Subsystem Vendor ID and Subsystem ID Registers

Subsystem Vendor ID and Subsystem ID are optional registers that are implemented in this design. Both registers are loaded from the serial EEPROM after RST#.

5.1.11 Interrupt Line Register

The Interrupt Line register is an eight bit register that is read/write. POST software will write the value of this register as it initializes and configures the system. The value in this register indicates which of the system interrupt controllers the device's interrupt pin is connected to.

5.1.12 Interrupt Pin Register

The Interrupt Pin register tells which interrupt pin the device uses. The value of this register will be 0x01, indicating that INTA# will be used.

5.1.13 Min Grant and Max Latency Registers

The Min Grant and Max Latency registers are used to specify the devices desired settings for Latency Timer values. For both registers, the value specifies a period of time in units of ¼ microsecond. Min Grant is used for specifying the desired burst period assuming a 33 MHz clock. Min Latency specifies how often the device needs to gain access to the PCI bus. These registers are loaded from the serial EEPROM after RST#.

5.2 BASE ADDRESS REGISTER

BIF provides a single Base Address Register. The Base Address Register is a 32 bit register that is used to access the BIF register set. Bits 3:0 are hard-wired to 0 to indicate memory space. Bits 15-4 will be hard-wired to 0. The remaining bits (31 - 16) will be read/write. This specifies that this device requires a 64k byte address space. After reset, the Base Address Register contains 0x00000000.

The 64k byte address space used by the BIF is divided into 4k byte regions. Each 4k byte region is used as Table 5-4.

Table 5-4. BIF Address Map

Address [15:12]	Address [11:0]	Region Name	Description
0x0	0x0-0xfff	BASIC2 Registers	Buffers, control, and status registers
0x1	0x0-0xfff	CIS Memory	Data loaded from Serial EEPROM for Card Bus applications
0x2	0x0-0xfff	DSP Scratch Pad	Access to DSP scratch page registers
0x3	0x0-0xfff	Reserved	
0x4	0x0-0xfff	Reserved	
0x5-0xf	0x0-0xfff	Reserved.	

5.3 SERIAL EEPROM INTERFACE

The serial EEPROM interface is used to load PCI configuration parameters and CIS information (required for Card Bus operation) after a reset occurs. The PCI configuration information to be loaded requires 10 bytes of data. The CIS information requires 384 bytes of data. The minimum serial EEPROM size is 512 bytes (4096 bits). After the PCI reset signal is negated, the configuration data is read from the serial EEPROM and stored in the PCI configuration registers as required, then the CIS information is read from the serial EEPROM and stored in the internal RAM of the BIF. While the serial EEPROM data is being read and is being loaded in the configuration registers and the CIS RAM, any PCI access that occurs will receive a RETRY signal from the BIF device. After completion of the serial EEPROM reads, the BIF device will accept PCI transactions.

The data stored in the serial EEPROM is in 16 bit word format. The configuration data to be read from the serial EEPROM is shown in Table 5-5.

Table 5-5. EEPROM Configuration Data

EEPROM Address	Copied to
0x0	Configuration Register Device ID
0x1	Configuration Register Vendor ID
0x2	Configuration Register Subsystem Device ID
0x3	Configuration Register Subsystem Vendor ID
0x4 (LSBs)	Configuration Register Min Grant
0x4 (MSBs)	Configuration Register Max Latency
Beyond 0x4	CIS RAM

6. COMMAND SET

The commands for the different models are listed by functional use in Table 6-1and alphanumerically in Table 6-2.

Table 6-1. Command Set Summary - Functional Use Sort

Command	Description	Configuration			
		Data/Fax	Data/Fax/Voice	Data/Fax/Voice/ Speakerphone	Data/Fax/Voice/ Speakerphone/ ISDN
	Generic Modem Control				
Z	Reset to Default Configuration	X	X	X	X
+FCLASS	Select Active Service Class	X	X	X	X
&F	Set to Factory-Defined Configuration	X	X	X	X
I	Request Identification Information	X	X	X	X
+GMI	Request Manufacturer Identification	X	X	X	X
+GMM	Request Model Identification	X	X	X	X
+GMR	Request Revision Identification	X	X	X	X
+GSN	Request Product Serial Number Identification	X	X	X	X
+GOI	Request Global Object Identification	X	X	X	X
+GCAP	Request Complete Capabilities List	X	X	X	X
	DTE-Modem Interface				
E	Command Echo	X	X	X	X
Q	Result Code Suppression	X	X	X	X
V	Modem Response Format	X	X	X	X
X	Result Code Selection and Call Progress Monitoring Control	X	X	X	X
&C	RLSD Behavior	X	X	X	X
&D	DTR Behavior	X	X	X	X
+IFC	DTE-Modem Local Flow Control	X	X	X	X
+ILRR	DTE-Modem Local Rate Reporting	X	X	X	X
+H	Enable/Disable Video Ready Mode	X	X	X	X
	Dial Control				
D	Dial	X	X	X	X
T	Select Tone Dial	X	X	X	X
P	Select Pulse Dial	X	X	X	X
A	Answer	X	X	X	X
H	Hook Control	X	X	X	X
O	Return to Online Data State	X	X	X	X
L	Monitor Speaker Loudness	X	X	X	X
M	Monitor Speaker Mode	X	X	X	X
&G	Select Guard Tone	X	X	X	X
&P	Select Pulse Dial Make/Break Ratio	X	X	X	X
&V	Display Current Configuration	X	X	X	X
&W	Store Current Configuration	X	X	X	X
	Modulation Control				
+MS	Modulation Selection	X	X	X	X
+MR	Modulation Reporting Control	X	X	X	X
	Error Control				
+ES	Error Control and Synchronous Mode Selection	X	X	X	X
+EB	Break Handling in Error Control operation	X	X	X	X
+ESR	Selective Repeat	X	X	X	X
+EFCS	32-bit Frame Check Sequence	X	X	X	X
+ER	Error Control Reporting	X	X	X	X
+ETBM	Call Termination Buffer Management	X	X	X	X

Table 5-1. Command Set Summary - Functional Use Sort (Cont'd)

Command	Description	Configuration			
		Data/Fax	Data/Fax/Voice	Data/Fax/Voice/ Speakerphone	Data/Fax/Voice/ Speakerphone/ ISDN
	Data Compression				
+DS	Data Compression	X	X	X	X
+DR	Data Compression Reporting	X	X	X	X
%E	Enable/Disable Line Quality Monitor and Auto-Retrain	X	X	X	X
%L	Line Signal Level	X	X	X	X
%Q	Line Signal Quality	X	X	X	X
	V.8 and V.8 bis				
+A8E	V.8 and V.8bis Operation Control	X	X	X	X
+A8M	Send V.8 Menu Signals	X	X	X	X
+A8T	Send V.8bis Signal and/or Message(s)	X	X	X	X
	Synchronous Mode Access				
+ESA	Synchronous Access Mode Configuration	X	X	X	X
+ITF	Transmit Flow Control Thresholds	X	X	X	X
	World-Class				
*B	Display Blacklisted Numbers	X	X	X	X
*D	Display Delayed Numbers	X	X	X	X
+GCI	Country of Installation	X	X	X	X
	DSVD Control				
-SSE	Enable/Disable DSVD	X	X	X	X
	Fax Commands				
+FAE	Data/fax Auto Answer	X	X	X	X
+FTS	Stop Transmission and Pause	X	X	X	X
+FRS	Wait for Silence	X	X	X	X
+FTM	Transmit Data with <MOD> Carrier	X	X	X	X
+FRM	Receive Data with <MOD> Carrier	X	X	X	X
+FTH	Transmit HDLC Data with <MOD> Carrier	X	X	X	X
+FRH	Receive HDLC Data with <MOD> Carrier	X	X	X	X
+FAR	Adaptive Reception Control	X	X	X	X
+FCL	Carrier Loss Timeout	X	X	X	X
+FDD	Double Escape Character Replacement Control	X	X	X	X
+FIT	DTE Inactivity Timeout	X	X	X	X
+FPR	Local DTE-Modem Serial Port Rate				
+FMI	Manufacturer Identification	-	X	X	X
+FMM	Product Identification	-	X	X	X
+FMR	Version, Revision, etc.	-	X	X	X
+FLO	Flow Control	-	X	X	X
	S-Parameters				
S0	Automatic Answer	X	X	X	X
S1	Ring Counter	X	X	X	X
S2	Escape Character	X	X	X	X
S3	Command Line Termination Character	X	X	X	X
S4	Response Formatting Character	X	X	X	X
S5	Command Line Editing Character	X	X	X	X
S6	Pause Before Blind Dialing	X	X	X	X
S7	Connection Completion Timeout	X	X	X	X
S8	Comma Dial Modifier Time	X	X	X	X
S10	Automatic Disconnect Delay	X	X	X	X
S11	DTMF Tone Duration	X	X	X	X
S12	Escape Prompt Delay (EPD)	X	X	X	X
S29	Flash Dial Modifier Time	X	X	X	X

Table 5-1. Command Set Summary - Functional Use Sort (Cont’d)

Command	Description	Configuration			
		Data/Fax	Data/Fax/Voice	Data/Fax/Voice/ Speakerphone	Data/Fax/Voice/ Speakerphone/ ISDN
	Voice Commands				
+VCID	Caller ID (CID)	-	X	X	X
+VDID	DID Feature	-	X	X	X
+VNH	Automatic Hang-up Control	-	X	X	X
+VIP	Voice Initialize All Parameters	-	X	X	X
+VRX	Start Modem Receive (Record)	-	X	X	X
+VTS	Voice Tone Send	-	X	X	X
+VTX	Start Modem Transmit (Playback)	-	X	X	X
+VGR	Voice Gain Receive (Record Gain)	-	X	X	X
+VGT	Voice Gain Transmit (Playback Volume)	-	X	X	X
+VIT	Voice Inactivity Timer (DTE/modem)	-	X	X	X
+VLS0-15	Analog Source/Destination Selection	-	X	X	X
+VRA	Ringback Goes Away Timer	-	X	X	X
+VRN	Ringback Never Appeared Timer	-	X	X	X
+VSD	Silence Detection (QUIET & SILENCE)	-	X	X	X
+VSM	Compression Method Selection	-	X	X	X
+VTD	Beep Tone Duration Timer	-	X	X	X
+VDR	Distinctive Ring	-	X	X	X
+VDT	Control Tone Cadence Reporting	-	X	X	X
+VBT	Buffer Threshold Setting	-	X	X	X
+VPR	Select DTE/Modem Interface Rate	-	X	X	X
	Speakerphone Commands				
+VSP	Speakerphone ON/OFF	-	-	X	X
+VDX	Speakerphone Duplex Mode	-	-	X	X
+VLS16-19	Speakerphone Signal Control	-	-	X	X
+VGM	Microphone Gain				
+VGS	Speaker Gain	-	-	X	X

Table 6-2. Command Set Summary - Alphanumeric Sort

Command	Description	Configuration			
		Data/Fax	Data/Fax/Voice	Data/Fax/Voice/ Speakerphone	Data/Fax/Voice/ Speakerphone/ ISDN
%E	Enable/Disable Line Quality Monitor and Auto-Retrain	X	X	X	X
%L	Line Signal Level	X	X	X	X
%Q	Line Signal Quality	X	X	X	X
&C	RLSD Behavior	X	X	X	X
&D	DTR Behavior	X	X	X	X
&F	Set to Factory-Defined Configuration	X	X	X	X
&G	Select Guard Tone	X	X	X	X
&P	Select Pulse Dial Make/Break Ratio	X	X	X	X
&V	Display Current Configuration	X	X	X	X
&W	Store Current Configuration	X	X	X	X
*B	Display Blacklisted Numbers	X	X	X	X
*D	Display Delayed Numbers	X	X	X	X
+A8E	V.8 and V.8bis Operation Control	X	X	X	X
+A8M	Send V.8 Menu Signals	X	X	X	X
+A8T	Send V.8bis Signal and/or Message(s)	X	X	X	X
+DR	Data Compression Reporting	X	X	X	X
+DS	Data Compression	X	X	X	X
+EB	Break Handling in Error Control operation	X	X	X	X
+EFCS	32-bit Frame Check Sequence	X	X	X	X
+ER	Error Control Reporting	X	X	X	X
+ES	Error Control and Synchronous Mode Selection	X	X	X	X
+ESA	Synchronous Access Mode Configuration	X	X	X	X
+ESR	Selective Repeat	X	X	X	X
+ETBM	Call Termination Buffer Management	X	X	X	X
+FAE	Data/fax Auto Answer	X	X	X	X
+FAR	Adaptive Reception Control	X	X	X	X
+FCL	Carrier Loss Timeout	X	X	X	X
+FCLASS	Select Active Service Class	X	X	X	X
+FDD	Double Escape Character Replacement Control	X	X	X	X
+FIT	DTE Inactivity Timeout	X	X	X	X
+FLO	Flow Control	-	X	X	X
+FMI	Manufacturer Identification	-	X	X	X
+FMM	Product Identification	-	X	X	X
+FMR	Version, Revision, etc.	-	X	X	X
+FPR	Local DTE-Modem Serial Port Rate	X	X	X	X
+FRH	Receive HDLC data with <MOD> carrier	X	X	X	X
+FRM	Receive Data with <MOD> carrier	X	X	X	X
+FRS	Wait for Silence	X	X	X	X
+FTH	Transmit HDLC data with <MOD> carrier	X	X	X	X
+FTM	Transmit Data with <MOD> carrier	X	X	X	X
+FTS	Stop Transmission and Pause	X	X	X	X
+GCAP	Request Complete Capabilities List	X	X	X	X
+GCI	Country of Installation	X	X	X	X
+GMI	Request Manufacturer Identification	X	X	X	X
+GMM	Request Model Identification	X	X	X	X
+GMR	Request Revision Identification	X	X	X	X
+GOI	Request Global Object Identification	X	X	X	X
+GSN	Request Product Serial Number Identification	X	X	X	X
+H	Enable/Disable Video Ready Mode	X	X	X	X

Table 5-2. Command Set Summary - Alphanumeric Sort (Cont'd)

Command	Description	Configuration			
		Data/Fax	Data/Fax/Voice	Data/Fax/Voice/ Speakerphone	Data/Fax/Voice/ Speakerphone/ ISDN
+IFC	DTE-Modem Local Flow Control	X	X	X	X
+ILRR	DTE-Modem Local Rate Reporting	X	X	X	X
+ITF	Transmit Flow Control Thresholds	X	X	X	X
+MR	Modulation Reporting Control	X	X	X	X
+MS	Modulation Selection	X	X	X	X
+VBT	Buffer Threshold Setting	-	X	X	X
+VCID	Caller ID (CID)	-	X	X	X
+VDID	DID Feature	-	X	X	X
+VDR	Distinctive Ring	-	X	X	X
+VDT	Control Tone Cadence Reporting	-	X	X	X
+VDX	Speakerphone Duplex Mode	-	-	X	X
+VGM	Microphone Gain	-	-	X	X
+VGR	Voice Gain Receive (Record Gain)	-	X	X	X
+VGS	Speaker Gain	-	-	X	X
+VGT	Voice Gain Transmit (Playback Volume)	-	X	X	X
+VIP	Voice Initialize All Parameters	-	X	X	X
+VIT	Voice Inactivity Timer (DTE/modem)	-	X	X	X
+VLS	Analog Source/Destination Selection	-	X	X	X
+VNH	Automatic Hang-up control	-	X	X	X
+VPR	Select DTE/Modem Interface Rate	-	X	X	X
+VRA	Ringback Goes Away Timer	-	X	X	X
+VRN	Ringback Never Appeared Timer	-	X	X	X
+VRX	Start Modem Receive (Record)	-	X	X	X
+VSD	Silence Detection (QUIET & SILENCE)	-	X	X	X
+VSM	Compression Method Selection	-	X	X	X
+VSP	Speakerphone ON/OFF	-	-	X	X
+VTD	Beep Tone Duration Timer	-	X	X	X
+VTS	Voice Tone Send	-	X	X	X
+VTX	Start Modem Transmit (Playback)	-	X	X	X
-SSE	Enable/Disable DSVD	X	X	X	X
A	Answer	X	X	X	X
D	Dial	X	X	X	X
E	Command Echo	X	X	X	X
H	Hook Control	X	X	X	X
I	Request Identification Information	X	X	X	X
L	Monitor Speaker Loudness	X	X	X	X
M	Monitor Speaker Mode	X	X	X	X
O	Return to Online Data State	X	X	X	X
P	Select Pulse Dial	X	X	X	X
Q	Result Code Suppression	X	X	X	X

Table 5-2. Command Set Summary - Alphanumeric Sort (Cont'd)

Command	Description	Configuration			
		1- Data/Fax	2- Plus Voice	3- Plus SP	5- Plus ISDN
S0	Number of Rings to Automatic Answer	X	X	X	X
S1	Ring Counter	X	X	X	X
S2	Escape Character	X	X	X	X
S3	Line Termination Character	X	X	X	X
S4	Response Formatting Character	X	X	X	X
S5	Command Line Editing Character	X	X	X	X
S6	Pause Before Blind Dialing	X	X	X	X
S7	Connection Completion Timeout	X	X	X	X
S8	Comma Dial Modifier Time	X	X	X	X
S10	Automatic Disconnect Delay	X	X	X	X
S11	DTMF Tone Duration	X	X	X	X
S12	Escape Prompt Delay (EPD)	X	X	X	X
S29	Flash Dial Modifier Time	X	X	X	X
T	Select Tone Dial	X	X	X	X
V	Modem Response Format	X	X	X	X
X	Result Code Selection and Call Progress Monitoring Control	X	X	X	X
Z	Reset To Default Configuration	X	X	X	X

NOTES

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